3. DXX CLUSTER NODE

3.1 Introduction

The DXX Cluster Node represents the largest node of the Ericsson DXX system. It is built in a master-slave architecture.

A Cluster Node is formed by connecting max. 8 single or double subracks (slave subracks) to the cluster master subrack (see Fig. 2).

One Cluster Node slave can be a single or double subrack node. Therefore, the maximum cross-connect capacity of a Cluster Node is 512 Mbit/s (8 x 64 Mbit/s, or 256 x 2 Mbit/s). Normally a Cluster Node is not equipped with channel interfaces. It is typically equipped with only 2 Mbit/s or 8 Mbit/s trunk interfaces. 64 kbit/s is the lowest speed which can be cross-connected in a Cluster Node.

The master subrack is always a double subrack. In this subrack are located the control and cross-connect units which control the whole Cluster Node. One cross-connect unit (CXU-A) is needed in the master subrack for each slave subrack. All CXU-As have redundancy.

There are six common logic units in a Cluster Node. These units are CCU, SCU, CXU-A, CXU-M, CXU-S, and SXU-C.

Cluster Nodes are used only with GMH or GMM interface units and the smallest cross-connect unit is a 64 kbit/s time slot and its four signalling bits. The maximum capacity of the cluster cross-connect node is 8 x 64 Mbit/s, for example 256 pcs 2 Mbit/s trunk lines.

All other characteristics of the Cluster Node are the same as for the Basic Node.

3.2 General

3.2.1 Master Subrack of the Cluster Node

The cluster master subrack consists of the following units:

Cluster Master Subrack Units for n Slave Subracks

Unit Type	Unit Name	Protected Configuration [a]
RXS-CD	Subrack	1 pc
PFU, PFU-A	Fuse unit	2 pcs
PFU-B	Fuse unit (battery protection)	2 pcs
CCU	Cluster control unit	1 pc
CXU-M	Cluster cross-connect unit/master	1 + 1 pcs
CXU-A	Cluster cross-connect unit/slave	n + n[b]
CXU-S	Signalling cross-connect unit	1 + 1 pcs

a Cross-Connection protected

b n = number of slave subracks

The battery power feeding of the Cluster Node can be protected by the PFU-B unit in each shelf. Note that this is only possible when the first fuse unit is PFU-A.

The equipped master subrack is given in Fig. 1.

The PFU fuse unit and its functions are the same as in the single subrack node. The RXS-CD subrack mechanics is similar to the RXS-D subrack but the mother boards and the bus extender cards are different.

The CCU control unit hardware is the same as in the the SCU control unit. The functions of the CCU control unit are similar to the SCU control unit but the processor program is different. The CCU communicates with the CXU-M units of the cluster master subrack via the internal control bus. The communication between the CCU unit and the SCU units of the slave subracks is done via the external control bus. The structure of this bus is similar to the internal control bus (2 Mbit/s Token bus) but the bit rate is 1 Mbit/s.

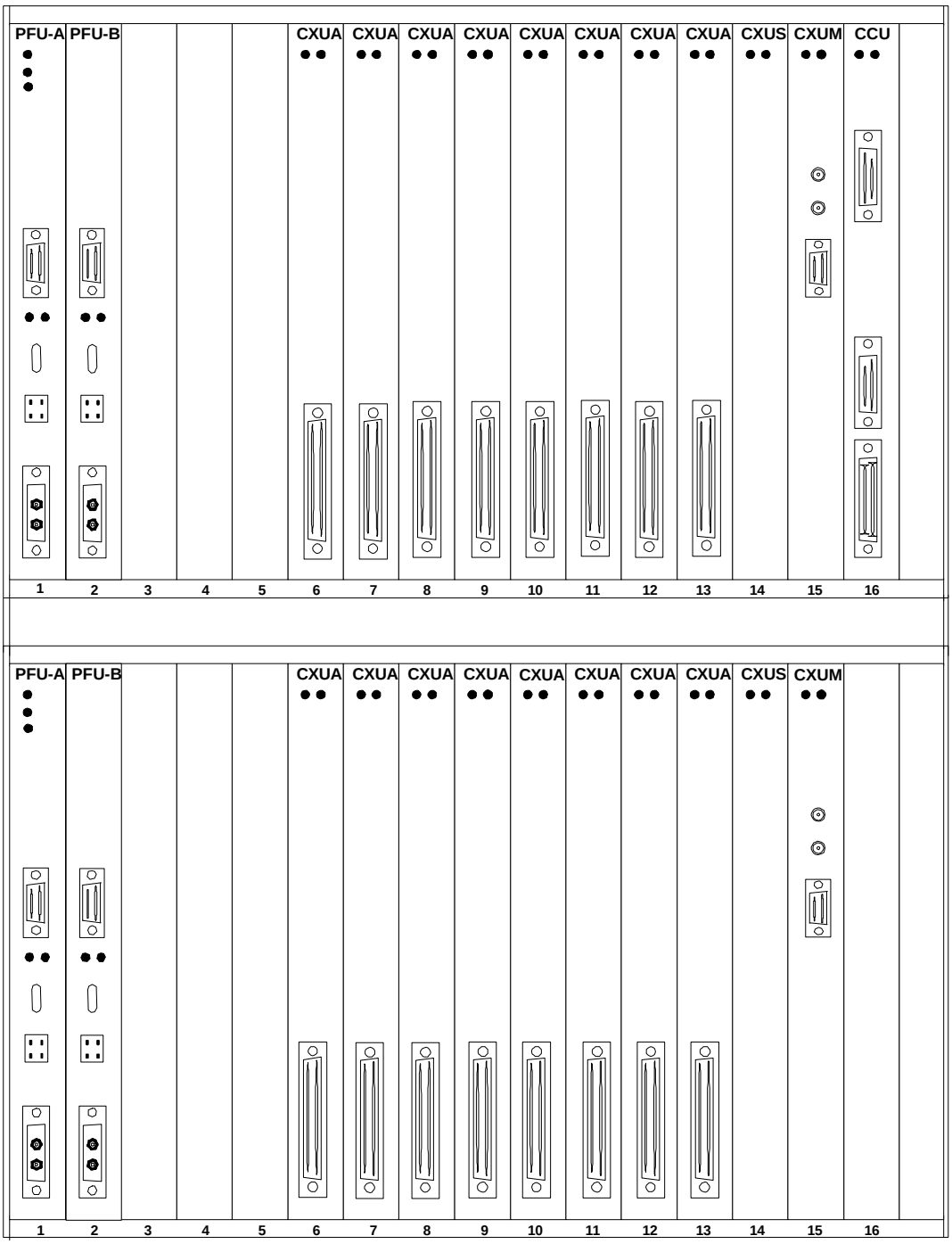


Fig. 1: Master Subrack of the Cluster Node

3.2.2 Slave Subracks of the Cluster Node

The units and the configuration of the slave subracks are basically the same as in the normal single or double subrack. The GMH or GMM interface units are connected to the cross-connect bus, and the SXU generates timing signals for the bus.

The SXU is no more responsible for the master clock of the node and the cross-connection between ports. Its function is to adapt the 64 Mbit/s cross-connection bus to the cluster master subrack.

The 64 Mbit/s X-bus is connected to the master subrack through an SXU-C unit. The smaller version of the SXU is used but it includes an intersubrack interface module through which the 64 Mbit/s bus is connected to the cluster master subrack. The cluster slave SXU has its own SW so that the name of this unit combination is SXU-C.

The actual cross-connection is done in the cluster master subrack even when the two cross-connected ports are in the same slave subrack.

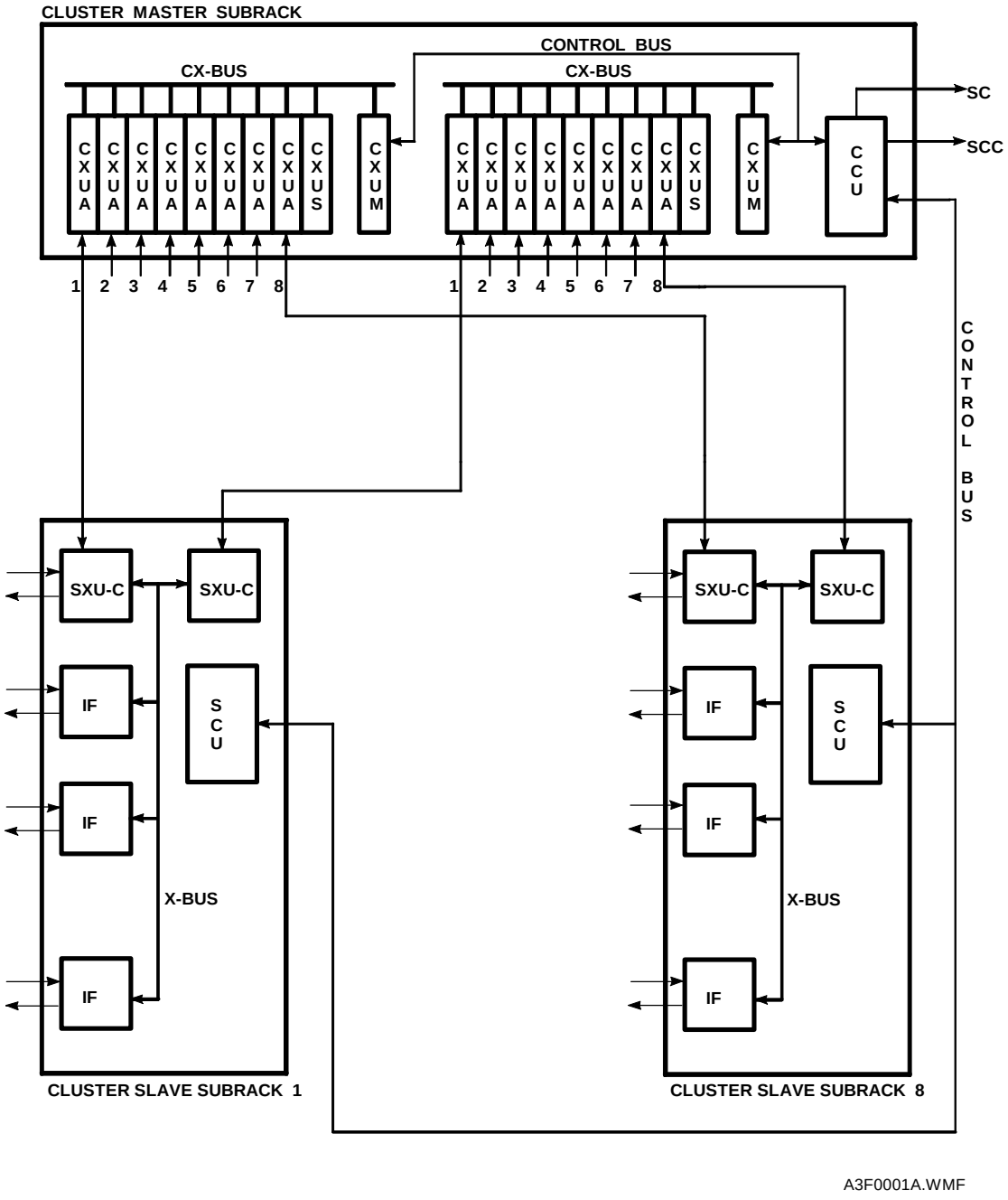


Fig. 2: Cluster Node

3.2.3 Cluster Cross-Connect Switch

The CXU-M is responsible for the control of cross-connections. The actual cross-connect switch is distributed into the CXU-A cross-connect units. They are interconnected by the cluster cross-connect bus (CX-bus).

The cross-connect switch for 8 slave subracks consists of:

— one CXU-A for each slave subrack
— one CXU-S unit for the cross-connection of signalling bits (XD-channel)
— one CXU-M unit for the control of the cross-connection

The master clock of the Cluster Node is in thea CXU-M unit. It has access to any interface receive clock in slave subracks in order to lock the master clock to the desired signal.

The functions of the master clock are the same as in the SXU unit:

— external clock input
— external clock output
— clock fallback list

Protected Cross-Connect

The cross-connect capacity of the Cluster Node is so big that the cross-connect part of the node is normally duplicated.

In this case the SXU-C units of the slave subracks are also duplicated. The second SXU-C is used to connect the slave subrack to the other cross-connect switch of the master subrack. The protecting part of the master subrack is in the lower shelf of the RXS-CD subrack. The protected cluster master subrack has only one CCU control unit which controls both CXU-M units. The control bus goes through the whole double subrack.

The two cross-connect switches operate totally independently. The change-over is done by the CXU units. This operation is controlled by the CCU unit.

3.3 Cluster Node Cross Connection

A Cluster Node consists of one cluster main subrack and of up to eight cluster slave subracks (DXX basic subracks) linked via intersubrack cables. Cross-connections are realized by the cluster main subrack, which contains a cross-connect matrix consisting of several units. The main subrack cannot contain node access units.

The subracks of a Cluster Node are placed in adjacent racks. A Cluster Node with eight slave subracks typically occupies three racks.

3.3.1 Node Capacity

The Cluster Node can accommodate 256 of 2048 kbit/s ports or 64 of 8448 kbit/s ports (total capacity is 512 Mbit/s). N x 64 kbit/s signals with possible channel associated signalling can be cross-connected. A strictly non-blocking time space matrix is implemented.

3.3.2 Main Subrack Cross-Connect Units

The cross-connect matrix consists of up to eight cluster cross-connect units CXU-A, one CXU-S signalling cross-connect unit (optional) and one CXU-M master cross-connect unit. In protected use the matrix is doubled for redundancy.

CXU-A cross-connects n x 64 kbit/s signals. CXU-A links to a slave subrack by an intersubrack cable.

CXU-S cross-connects n x 0.5 kbit/s signals multiplexed by the multiframe. CXU-S is common for the eight slave subracks. It has no external interface to the slave subracks.

Cluster cross-connect unit CXU-M supervises the operation of CXU-As and CXU-S and supplies bus timing in the main subrack. CXU-M receives cross-connection commands and maintains the cross-connect memories of CXU-A/CXU-S.

3.3.3 Slave Subrack Cross-Connect Unit

The basic subrack's hardware is adapted for cluster operation by replacing the cross-connect unit SXU-A/B with the variation SXU-C (see SXU description). The SXU-C is similar to the SXU-A but provided with an intersubrack interface module and a program memory for cluster operation. The SXU-C does not do actual cross-connection, it only transfers signals to/from the main subrack.

3.3.4 Main Subrack Cross-Connect Bus

The cross-connect bus (CX-bus) covers unit positions 6 to 14 (15) in the main subrack's back plane. The CX-buses in the two shelves of a subrack are not interconnected.

CXU-M supplies the bus clock (16896 kHz), the frame timing (8 kHz) and the multiframe timing (0.5 kHz). CXU-As synchronize to the bus timing.

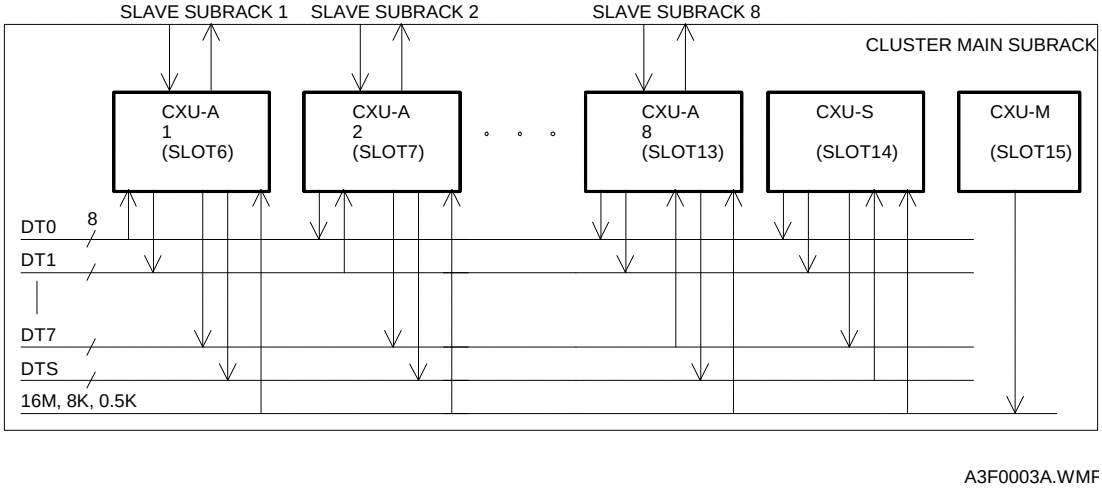


Fig. 3: CX-Bus Structure and the Cross-Connect Units

Physical Structure

One eight-bit wide databus (DT) is implemented for each CXU-A. Each DT-bus has a capacity of 1056 x 64 kbit/s (67 584 kbit/s).

A CXU-A can output a cross-connected byte to any DT-bus. The contents of each DT-bus are transferred by a particular CXU-A to the respective slave subrack. Bus congestion cannot occur.

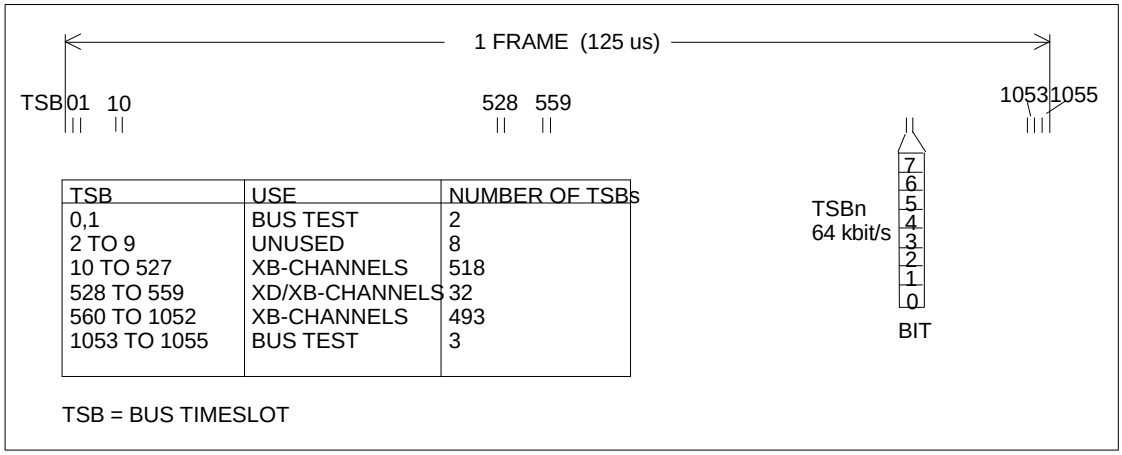
A common signalling bus (DTS) is provided for transferring XD-signals from CXU-As to the CXU-S. The cross-connected XD-signal is connected from the CXU-S to any DT-bus.

Logical Division

The DT-bus is divided into 1056 time slots (TS) numbered from 0 to 1055. Each TS represents a 64 kbit/s signal capacity.

32 time slots on a DT-bus can be multiplexed by the 16 frames long multiframe producing channel rates at n x 0.5 kbit/s.

Five time slots are reserved for node internal testing leaving 1051 TSs for cross-connected signals. Whole time slots are always transferred on the bus.



TSB	USE	NUMBER OF TSBs
0,1	BUS TEST	2
2 TO 9	UNUSED	8
10 TO 527	XB-CHANNELS	518
528 TO 559	XD/XB-CHANNELS	32
560 TO 1052	XB-CHANNELS	493
1053 TO 1055	BUS TEST	3

Fig. 4: CX Bus Logical Structure

CX-Bus Allocation

The slave subrack SXU-C allocates its X-bus independently as in a Basic Node (described in the Cross-Connect Unit SXU)). The CX-bus follows the X-bus allocation. CXU-M polls the allocation from each SXU-C and creates cross-connections accordingly.

3.3.5 Intersubrack Cross-Connect Bus

CXU-A is linked to the respective SXU-C via an intersubrack cross-connect bus (IS-bus). A slave subrack transfers data received by its interface units via the IS-bus to the main subrack for cross-connection. Cross-connected signals are then transferred via the IS-bus back to the slave subrack.

The frame structure of the IS-bus is similar to that of the CX-bus. 64 Mbit/s is transmitted in both directions by four data lines along with a clock and a frame/multiframe phase line.

Symmetrical pairs are used with V.11 electrical levels. Cables are supplied at a couple of lengths. The maximum length is 10 meters.

3.3.6 XB Signal Path in a Cluster Node

Fig. 5 shows an example of the signal path (dashed line) from slave subrack 1 to slave subrack 2.

An IF unit in slave subrack 1 transfers its received line signal to a buffer memory (BM). If the minimum length buffer is selected, the average signal delay in the buffer is one frame (125 ms) with a possible variation of + 1 frame. From the BM the signal goes to the X-bus and via the SXU-C to the CXU-A/1 without any significant delay.

In CXU-A/1 the signal is stored in a memory (XM), and in the next frame cross-connected via DT1 to CXU-A/2. The signal delay is one frame on the average.

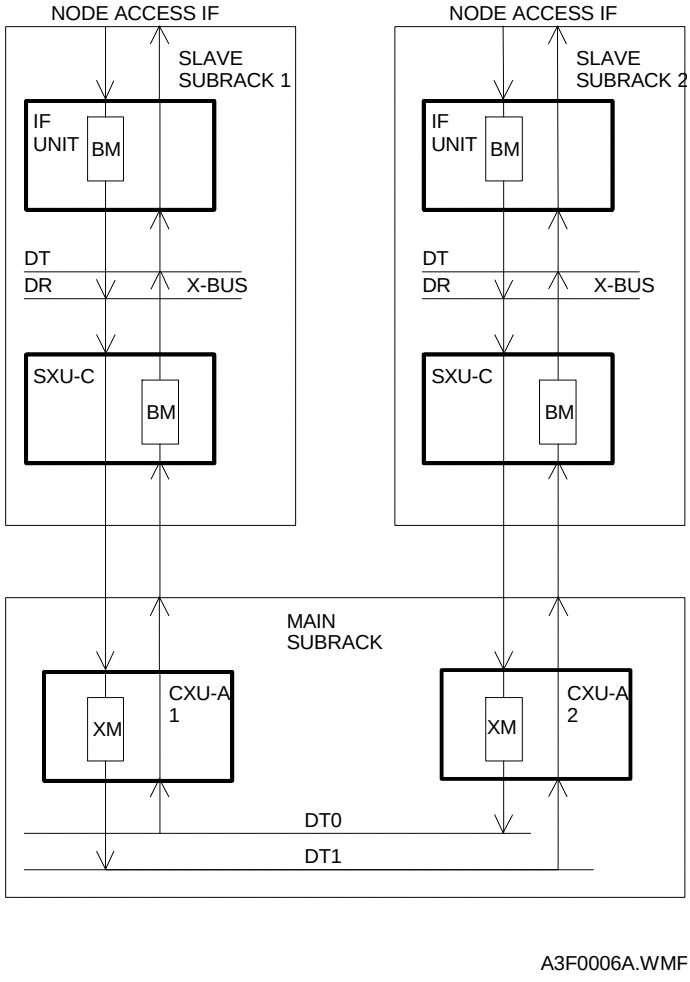


Fig. 5: XB Signal Path

CXU-A/2 sends the signal directly to the SXU-C in slave subrack 2. In SXU-C the signal is stored in a buffer memory and transferred to the X-bus. SXU-C delays the signal for nearly one frame.

The buffer in the transmit direction in the IF-unit is very short (if minimum receive buffer is chosen).

The total delay for X signals is in the order of three frames (375 ms). The cluster main subrack adds a delay of one frame when compared to the basic subrack.

Frame Phase Control

The frame phase in a Cluster Node is generated in the CXU-M unit, from where it is distributed to the CXU-A units (in a protected main subrack both shelves have an independent phase).

CXU-A transfers the phase to the slave subrack's SXU-C, which adjusts its frame phase to be somewhat ahead of the main subrack's phase. This enables the phase of the signal coming into the CXU-A to be delayed to match the CX-bus phase.

3.3.7 XD Signal Path

XD-signals and XB-signals are handled in separate buffer memories in IF units and in the cluster main subrack. In the SXU-C unit XD-signals are not separated from the XB-signals.

An IF-unit with a minimum length XB-buffer also has a minimum length XD-buffer, which, on the average, is one multiframe long. IF units in the Cluster Node apply a special multiframe phase mode, in which the IF-unit shifts its multiframe phase in the transmit direction one frame behind the multiframe phase in the receive direction. This shift compensates for the additional delay of one frame within the SXU-C buffer.

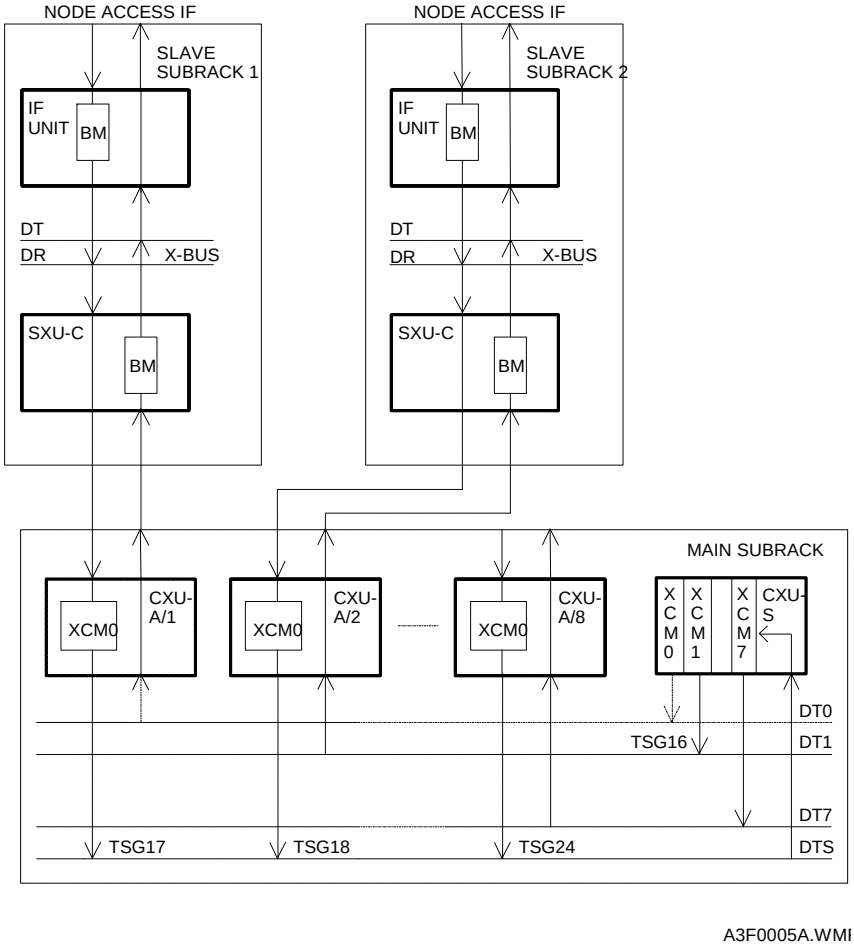


Fig. 6: XD Signal Path

In the main subrack XD time slots are temporarily stored in the cross-connect matrix 0 (XCM0). This is implemented in order to multiplex XD-signals from eight CXU-As onto one bus. XCM0 gives the XD TSs to the DTS-bus in a burst of 32 time slots. Buffering introduces an insignificantly small delay.

In the CXU-S each XCM stores DTS-bus bytes in a two multiframe long buffer memory. In the next frame 32 bytes are cross-connected bit-by-bit and sent to the respective DT-bus in TSB 528…559 (TSG16). The signal multiframe phase is delayed one frame within the SXU-C.

The total delay for XD-signals in the Cluster Node is three multiframes (6 ms) on the average. The additional delay as compared to a Basic Node is one multiframe.

3.3.8 Cluster Node Clock System

The network clock is supplied to the Cluster Node via redundant ports in the cluster slave subracks. External clock interfaces in the CXU-M and in the SXU-C can also be employed.

Two clock signals in each slave subrack can be connected to the subrack's SYNC BUS 1/2 and transferred via the intersubrack cable to the respective CXU-A. CXU-A buffers clocks according to the fallback list to the CLUSTER SYNC BUS 1/2 and to the CXU-M.

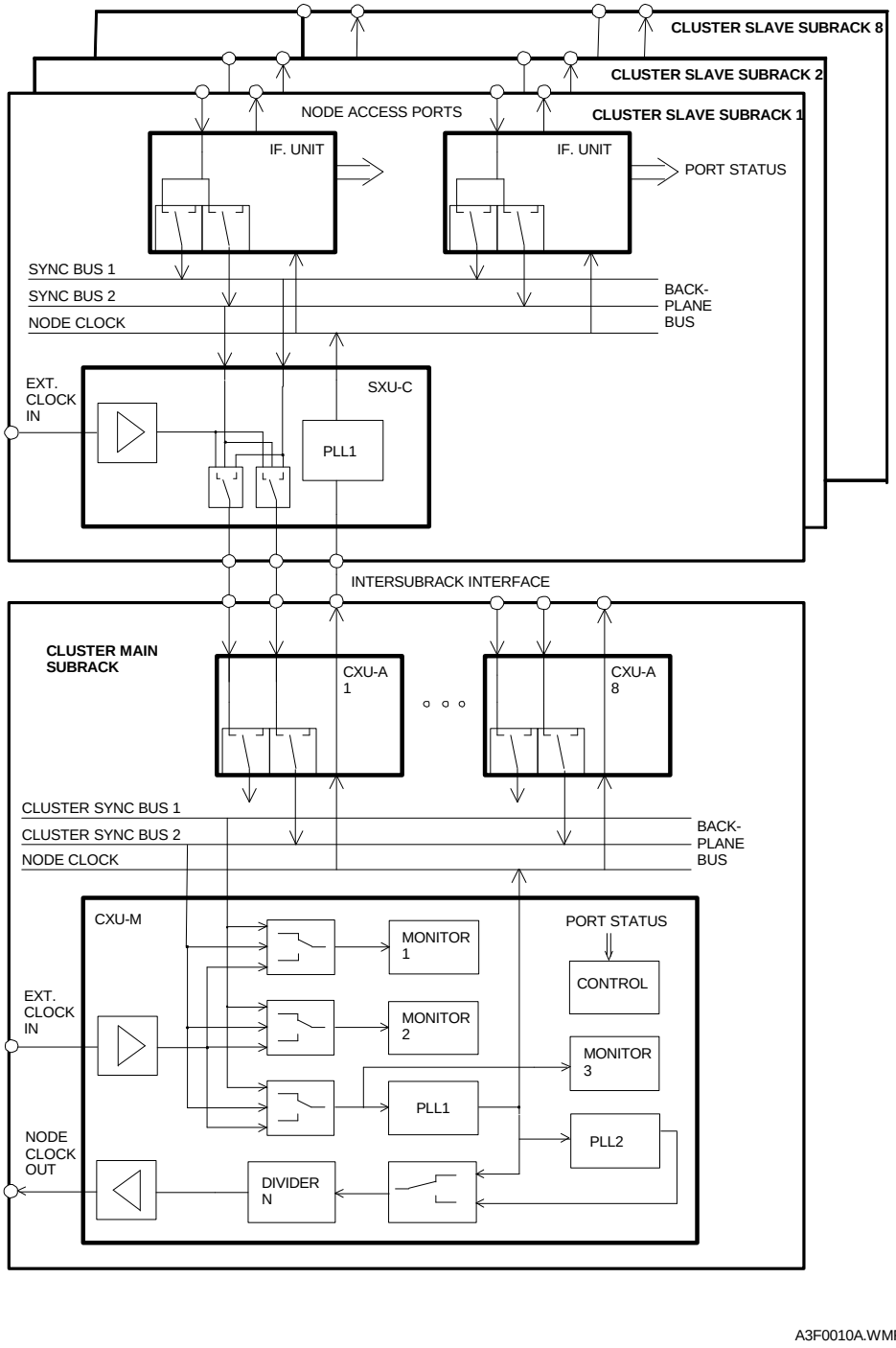


Fig. 7: Clock System Block Diagram

The Quality Level (QL) of Clock Signal

Each synchronization source (external clock interface or trunk line) has a parameter called Quality level and it has been defined as numerical values from 1 to 7 where 1 is the highest and 6 the lowest one (7 means ‘don’t use this clock’; used to prevent timing loops). The quality level of external clock is parametrizable for each node separately through NMS Master Clock window. (Usually value 1 is used.) The quality level of a clock obtained from trunk line is determined in the node where the clock originates. (In PDH network, it is usually 1 if the original source is an external clock and 6 if the original source should be the internal clock of some node.) If a node should lose other clock sources and fall to internal clock, the quality level value is the one parameterized for internal clock in NMS Master Clock window (usually value 6 is used).

For PDH trunks such as GMH, the quality level is transmitted over the network via Neighbor Node Monitoring messages. For SDH trunks such as GMU, there is a mapping between the SSM (Synchronization Status Message) quality levels used in SDH networks and the proprietary Ericsson DXX quality levels, as follows.

SDH quality level	Interpretation in Ericsson DXX
QL-PRC	1
QL-SSU-T	2
QL-SSU-L	4
QL-SEC	5
QL-DNU	7

Ericsson DXX quality level	Interpretation for SDH
1	QL-PRC
2	QL-SSU-T
3	QL-SSU-L
4	QL-SSU-L
5	QL-SEC
6	QL-SEC
7	QL-DNU

Quality levels can be disabled through NMS Master Clock window, which means that the quality levels are ignored when selecting the node clock.

Quality Level Message Delays in Cluster Node

The distribution method of the quality level of a clock is different for SDH and PDH parts of the network, and so are the distribution delays.

In SDH trunks (for example, STM-1 interfaces in GMU units) the quality level is continuously transmitted in SSM messages in the SOH bytes of an STM-1 (ITU-T Recommendation G.707). The cross-connection unit, which controls the clock, exchanges the SSM messages through the cross-connection bus, which is a fast method. Consequently, the delay for passing an SSM message on to another node is short and depends mostly on data processing delay in the cross-connection unit. For SDH trunks, it less than 450 ms.

In PDH trunks (such as trunks between GMH units), the quality level is repeatedly sent to the far end using neighbour node messages (NNM). The interval between two NNM messages may depend on the trunk unit type, but it is typically 1 s. The cross-connection unit polls each trunk unit frequently, sends the current quality level, and receives the incoming quality levels. The delay between two polls of a single unit depends on the node type (cluster or basic).

Consequently, the delay for passing a quality level message on to another node through PDH trunks is the sum of three values: the polling delay for the incoming trunk unit, the polling delay for the outgoing trunk unit, and the delay in the NNM process of a trunk unit. All three delays are random, and their maximum values are as follows:

1. Polling delay for PDH units: max 7 s in cluster nodes.
2. NNM process delay for PDH trunks: max 1 s.

Average values can be estimated by dividing these three values by two. For example, the average delay between two GMH trunks in a cluster node might be 3.5 + 3.5 + 0.5 s = 7.5 s.

Fallback List

The operator selects in the Master Clock menu ports onto the fallback list and assigns their priority. Five clocks can be entered. CXU-M selects the highest priority clock with a good status for the PLL1, which gives the node clock. The node clock is sent back to each slave subrack, where SXU-C's oscillator locks into the node clock.

Among the clocks in the fallback list, the clock signal which has the highest quality level and the status of which is OK, is the one to which the master clock is synchronized. If clock signals have the same QL, the clock to which the master clock is synchronized is the one with the highest priority according to the Fallback list. However, if quality levels are disabled (see the previous section), all clocks are considered to have the same quality level. If no clock in fallback list is usable, the node uses the internal clock of CXU-M.

Clock Monitoring

CXU-M monitors the clock selected and the next choice on the fallback list. The external clock is monitored when enabled.

By a major fault in an IF unit port signal the IF unit clamps the clock to SYNC BUS 1/2 and sends a clock status message to the CXU-M. CXU-M's monitoring circuit then opens the phase-locked-loop maintaining the clock frequency until the processor selects another input to the PLL1. Internal timing is selected if all clocks on the fallback list have failed.

After a fault is removed the IF unit gradually clears the clock status. The operator can enter a clock acceptance time in the Master Clock menu. A clock is not selected again until its status has been good over the acceptance time.

The CXU-M supervises that the main oscillator is locked to the clock supplied by the IF unit. A phase-locked loop alarm is generated if the PLL can not lock, or if the clock contains excessive jitter.

Clock Faults Monitored in the CXU-M (software version 2.6 or earlier)

Fault Description	Status	LED	Alarm Message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Red	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Red	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yellow	Clock far end alarm

NOTE! ***Faults which light red LED cause protection switch to the redundant SXUs (unless the redundant SXUs have the same problem).***

Clock Faults Monitored in the CXU-M (software versions 2.7 to 2.8)

Fault Description	Status	LED	Alarm Message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Yellow	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Yellow	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yellow	Clock far end alarm
Faulty clock source (individual for each link); see description below	MEI	Yellow	Faulty clock source
SSM clock quality parameter from an SDH interface in unstable	MEI	Yellow	Unstable SSM

NOTE!

None of these faults causes protection switch. In particular, if the active CXU-M loses external clock but the redundant CXU-M does not, the node cannot utilize the external clock at all.

Clock Faults Monitored in the CXU-M (software version 2.9 and later)

Fault Description	Status	LED	Alarm Message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock enabled and missing	PMA	Yellow	Loss of external clock
External clock on fallback list, clock interface disabled	MEI	-	External clock warning
Locking to a clock failed: input frequency out of tolerance range (typically external clock)	PMA	Yellow	Phase-locked-loop alarm
Clock far end alarm (individual for each link)	MEI	Yellow	Clock far end alarm
Faulty clock source (individual for each link); see description below	MEI	Yellow	Faulty clock source
SSM clock quality parameter from an SDH interface in unstable	MEI	Yellow	Unstable SSM
External clock on fallback list but missing, and no other OK clock available	PMA	Red	Clock failure switchover

NOTE!

Faults which light red LED cause protection switch to the redundant SXUs (unless the redundant SXUs have the same problem).

If the node clock supplied by the SXU should fail, the GMH-units transmit an independent clock with a basic frequency tolerance to the output ports. Node clock alarm is generated by the IF unit.

If the node clock provided by the main subrack should fail, SXU-C supplies an independent clock for the slave subrack.

Faulty Clock Source Alarm

In software versions 2.7 and later, the following handling of phase-locked-loop problems is implemented.

Typically the actual problem is that the frequency of external clock input of the node is distorted so much as to exceed the tolerance of the phase-locked loop controlling the master clock. If such a problem is persistent, the clock source is marked as faulty, and the 'faulty clock source' alarm for that entry in the fallback list is raised. A clock which is marked as faulty cannot be used as the master clock of the node. When the network operation has fixed the original problem, it is necessary to reset the 'faulty clock source' alarm through NMS. This is done by updating the fallback list thorough NMS Master Clock window.

As the faulty clock source alarm prohibits further use of the clock without human intervention, it is implemented so that the alarm is not raised if the problem appears to be only temporary. Fig. 8 describes how the alarm is raised. There is a counter (cnt) which is zero if the clock has not had phase-locked loop problems recently and increases if problems appear. If the counter grows too high, the alarm is raised.

Note that is States 1 and 2 the clock is considered usable, and in States 3 and 4, unusable.

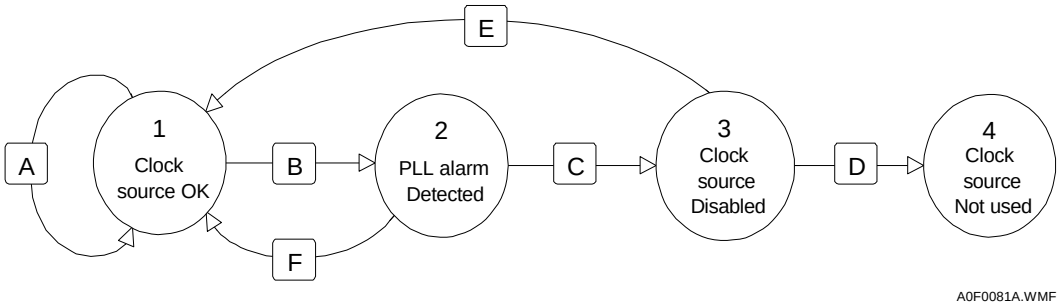


Fig. 8: Clock source

A - If cnt > 0 and no faults has occured for 5 minutes cnt is decremented by 1

B - PLL alarm occurs and cnt is incremented by one

C - PLL alarm on for more than 10 s

D - If cnt > 2 clock source is disabled permanently after 60 s (Until it is enabled from NMS)

E - If cnt < 3 clock source is enabled again after 60 s.

F - No PLL alarm during 10 s

Clock Far End Alarm

2 Mbit/s and 8 Mbit/s interfaces with a frame structure can employ a dedicated bit in the frame as a clock far end alarm bit (FEA). It can be used on links transferring network timing between nodes. If an intermediate node loses its synchronization to the network, the alarm bit is transmitted from all interfaces. A receiving node's IF unit, if on the fallback list, then produces a similar sequence for the clock as in a major fault of the incoming signal.

Clock Output Interface

Node clock output is provided at the external interface in the CXU-M and the SXU-Cs. The output is activated and its frequency selected from the Master Clock window of each subrack. The output control function can be activated in the master subrack only. If the output control is on, the clock output is disabled when the node clock uses internal timing or the external clock input. If the output control is off, clock output is active independently of the state of the fallback list.

3.3.9 Fault Monitoring

Main Subrack Tests

Cross-connect busses in use (DT0…7 and DTS) are surveyed by the CXU-M as a background process. The test also covers CXU-A's bus interface circuits and cross-connect matrices. Every bus test includes up to seven test elements depending on the number of installed CXU-As.

A test element comprises one receiving CXU-A and one sending CXU-A whose number is incremented during the test. The CXU-M creates a test cross-connection into TSB1054 using two alternating patterns and reads the received byte. shows one test element (dashed line) for DT1-bus from CXU-A/1 (sending unit) to CXU-A/2 (receiving unit).

A similar test is applied for the DTS-bus and the CXU-S.

Intersubrack IS-Bus Test

The cross-connect data links between the main subrack and the slave subracks are tested by the CXU-M and the SXU-C. Each SXU-C sends a test byte in one of the test time slots to the respective CXU-A, which loops the byte back. Similarly, each CXU-A sends a test byte to SXU-C, which loops the byte back.

Slave Subrack Test

The slave subrack busses and IF units are tested as described in the Basic Node description.

Fault Description	Status	LED	Alarm Message
DT-bus fault, CXU-A 1 to 8	PMA+S	Red	DT-bus fault
DTS-bus fault	PMA+S	Red	DTS-bus fault
IS-bus fault, bus 1 to 8	PMA+S	Red	IS-bus fault

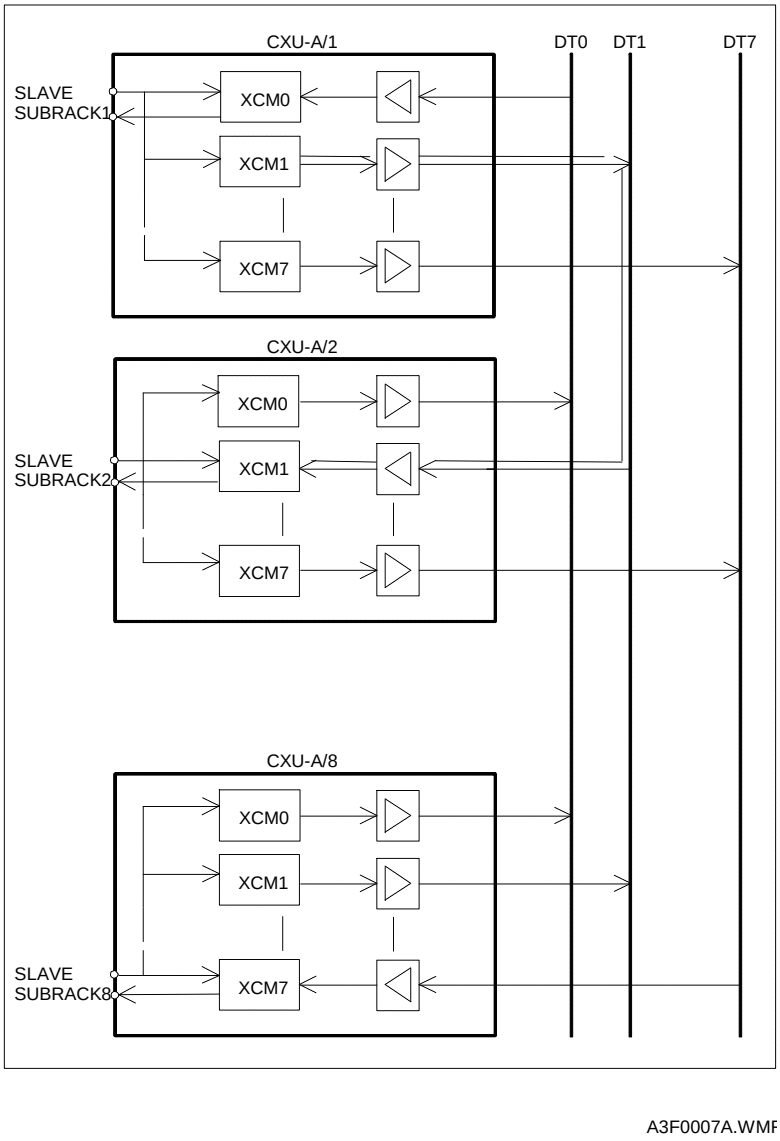


Fig. 9: DT-Bus Test Element

3.3.10 Cluster Node Protection

The Cluster Node is protected by duplicating the cross-connect units in the main subrack and the slave subracks. The two shelves of the cluster main subrack are independent with only the VTP control bus extending between the shelves.

The control unit CCU communicates with the two CXU-Ms, which receive the same control and cross-connection messages. Both sides cross-connect simultaneously. The passive SXU-Cs are disabled from the slave subrack X-bus.

CCU controls the switch-over based on CXU-M's response to polls and subrack alarm status. In a red alarm the SXU-Cs are switched. The cross-connected signal is first clamped, then the SXU-Cs are switched and the signal is enabled again .

3.4 Cluster Node Control Unit (CCU)

3.4.1 General

3.4.1.1 CCU Mechanical Design

The structure of the CCU unit is based on the standard mechanics of the DXX system. The width of the unit is 5T or one card slot in a DXX subrack. Card slot #16 (on the upper shelf of a double subrack node) is reserved for the CCU unit.

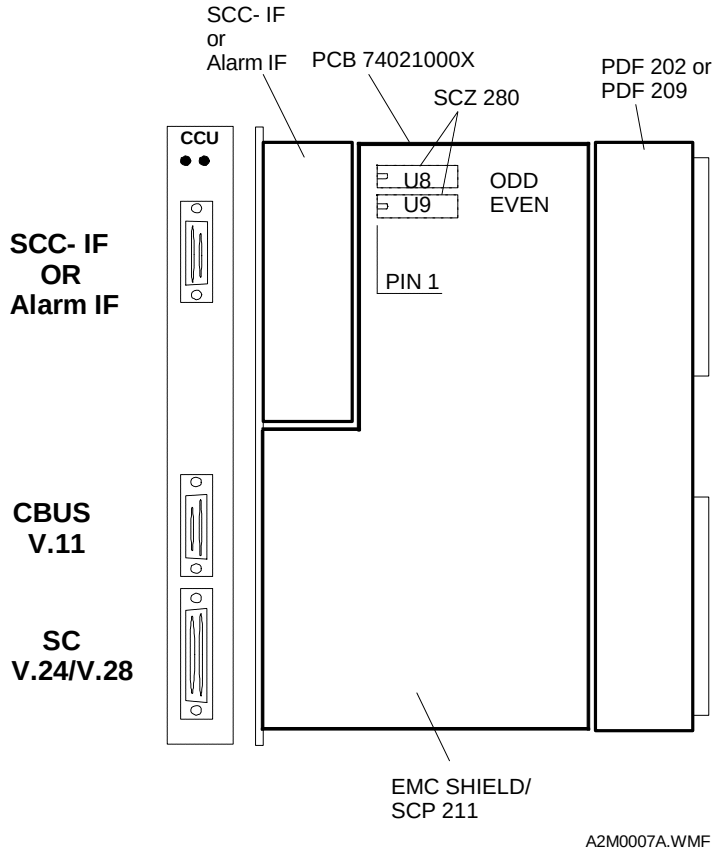


Fig. 10: CCU Unit Equipped with SCC-IF/Alarm-IF Module

The CCU unit needs to operate one piggy-back power supply unit PDF 202 or PDF 209 and two EPROMs with SCZ 286 program. The SCC X.25 interface module SCC-IF and the alarm interface module ALARM-IF are options which can be installed in the same manner as a normal interface piggy-back module of the DXX system.

Starting from the upper edge of the front panel of the unit, there are two alarm LEDs, one SCC connector or one alarm interface connector (D9 female), one CBUS connector and, lowest, the SC connector. On the back side of the unit there are two 2 x 32 pin eurocard (DIN 41612) connectors. The upper connector is used in transmitting the LOCAL VTP bus signals, the equipment alarm output signals, the 5 V power to the bus interface circuits and test input/output signals. The lower connector is used in transmitting the cross-connect bus signals, the 5 V power to the bus interface circuits and the battery bus.

3.4.2 Operation

3.4.2.1 CCU Block Diagram

The main functions of the CCU unit are the power supply, the microprocessor with its auxiliary circuits, the test signal Tx/Rx generator inside the IFMOD ASIC, the additional HDLC control channels option and the cross-connect bus interface.

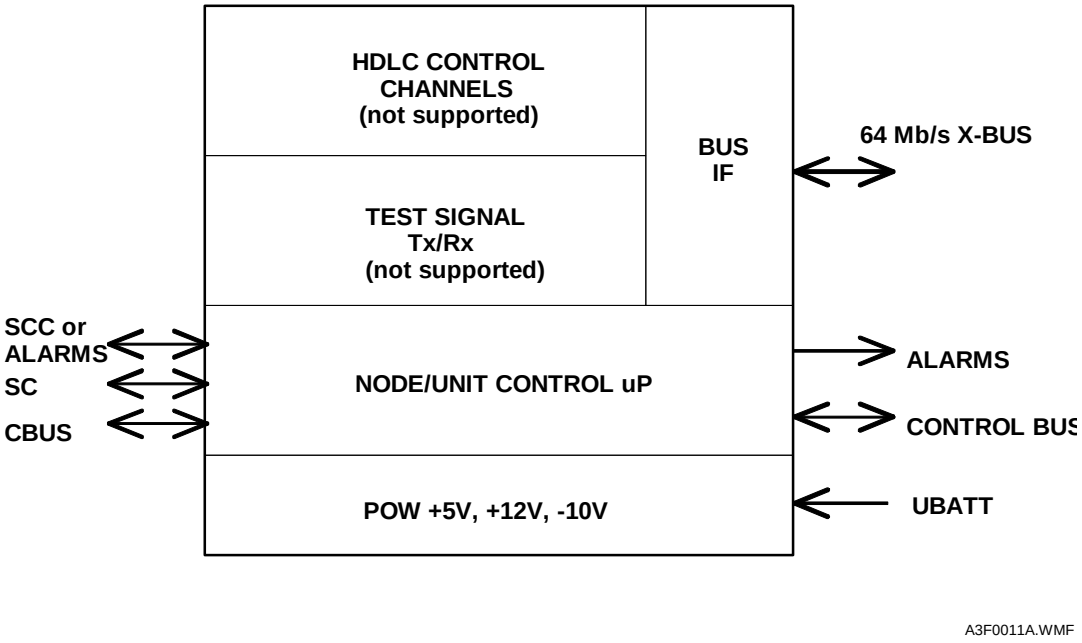


Fig. 11: CCU Block Diagram

Power Supply

The power supply delivers the operating voltages of the CCU unit from the battery bus voltage. The operating voltages are monitored by the microprocessor and if there is a failure, an alarm message is generated.

CCU Microprocessor

The detailed block diagram from the node/unit control block shows how the microprocessor controls and monitors the operation of the unit.

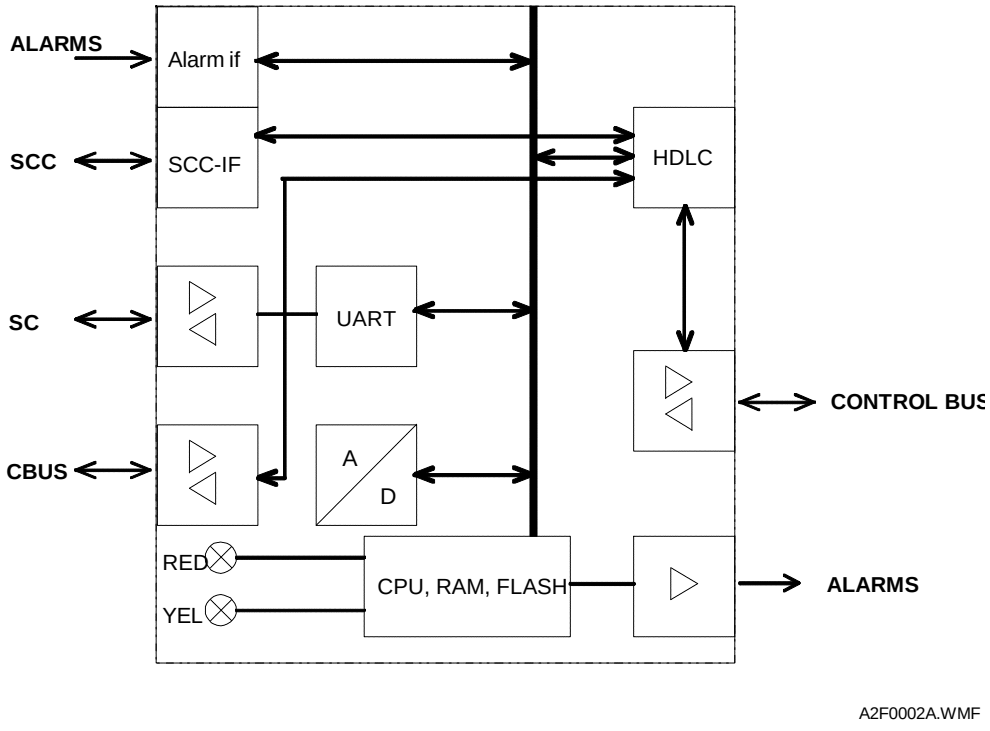


Fig. 12: Node/Unit Control Microprocessor

The microprocessor of the CCU unit is a 16-bit CMOS 80C186-16. It has three internal timers; two DMA channels; an interrupt controller; programmable memory and peripheral chip select logic; a programmable wait state generator and a local bus controller. It supports system level testing (ONCE test mode).

The microprocessor is upward compatible with 8086 and 8088 software and fully compatible with 80186 and 80188 software. It has two major modes of operation, compatible and enhanced. In compatible mode the microprocessor is completely compatible with NMOS 80186, with the of exception of 8087 support. The features of the enhanced mode are power-save control; dynamic RAM refresh and an asynchronous numeric coprocessor interface. The enhanced mode is used in the CCU unit.

Memory

Memory is implemented with six 32-pin surface mount components providing:

— 256 kBytes RAM (U15, 16)
— 512 kBytes FLASH PROM in two banks (U10, 11, 12 and 13)
— 256 kBytes of EPROM in two DIP packages (U8, 9)

HDLC Channels

The CCU unit has two pieces of dual channel synchronous serial controllers (SAB 82525, U48 and 49) providing:

— one LOCAL VTP bus interface (internal control bus) at 2 Mbit/s with advanced CMOS drivers (euro connector CN1)
— one CLUSTER VTP bus interface (external control bus) (CBUS connector CNF2) at 1024/512 kbit/s with V11 drivers
— two full duplex HDLC channels at up to 64 kbit/s, compliant with a subset of LAPB standard. Channel A is reserved for production testing phase. Channel B is used for communication with the NMS computer through SCC port (SCC-IF).

NOTE! ***The single-channel version of the communication controller is used in the place of U49 (SAB 82526) starting from hardware version 3.0.***

A/D Converter

The CCU unit has an 8-bit CMOS A/D converter with an 8-channel multiplexer. The A/D converter is used in supervising the operating voltages of the CCU unit and the BUS1 and BUS2 voltages of the cluster subrack.

SC Interface

The CCU unit has a single asynchronous serial channel. This interface is used on service computer connection (CNF1). The baud rate of the UART U14 (82510) can be selected from 300 baud to 19.2 k. The unit software sets the baud rate into 9600.

SCC Interface/Alarm Interface

On the unit there is one 2 x 10 pin header connector (CN4) for the SCC-IF X.25/V.11 interface module. The SCC-IF can be replaced by alarm interface module ALARM-IF. This module can be used to collect the alarms from battery backup system BBS into the DXX network.

Cross-Connect Interface

Unit has an interface to the 64 Mb/s cross-connect bus through CN5. The unit utilizes bus timing signals C16M, CLF and CLM, which are supplied by the SXU. The SXU changes data between SCU by transmitting the channel address which activates the data buffers in CIF ASIC. Both the received and transmitted data is transferred through their own 8-bit wide buses. The received data bus DR1 is protected by DR2.

3.4.2.2 Internal Control Buses

The CCU/SCU unit has interfaces for two internal control buses - the local VTP bus and the cluster VTP bus. The local VTP bus is used for communication between the units within one subrack and the cluster VTP bus is used for communication between the subracks of a Cluster Node. Both buses are synchronous serial high-speed local area networks with physically duplicated data, clock lines and interface circuits. The bit rate of the local VTP bus is 2 Mbit/s. The bit rate of the cluster VTP is 1 Mbit/s.

VTP is an abbreviation of the words Virtual Token Protocol which is a collision-free media access method based on the token passing principle implemented by the aid of timers. The logical link control is based on LLC3 protocol in both buses. The upper layer protocols are the same as the protocols of the external management interfaces of DXX nodes. The local VTP bus supports unit addresses 1…31. The cluster VTP bus supports subrack addresses 1…9. The locations of the control buses are shown below.

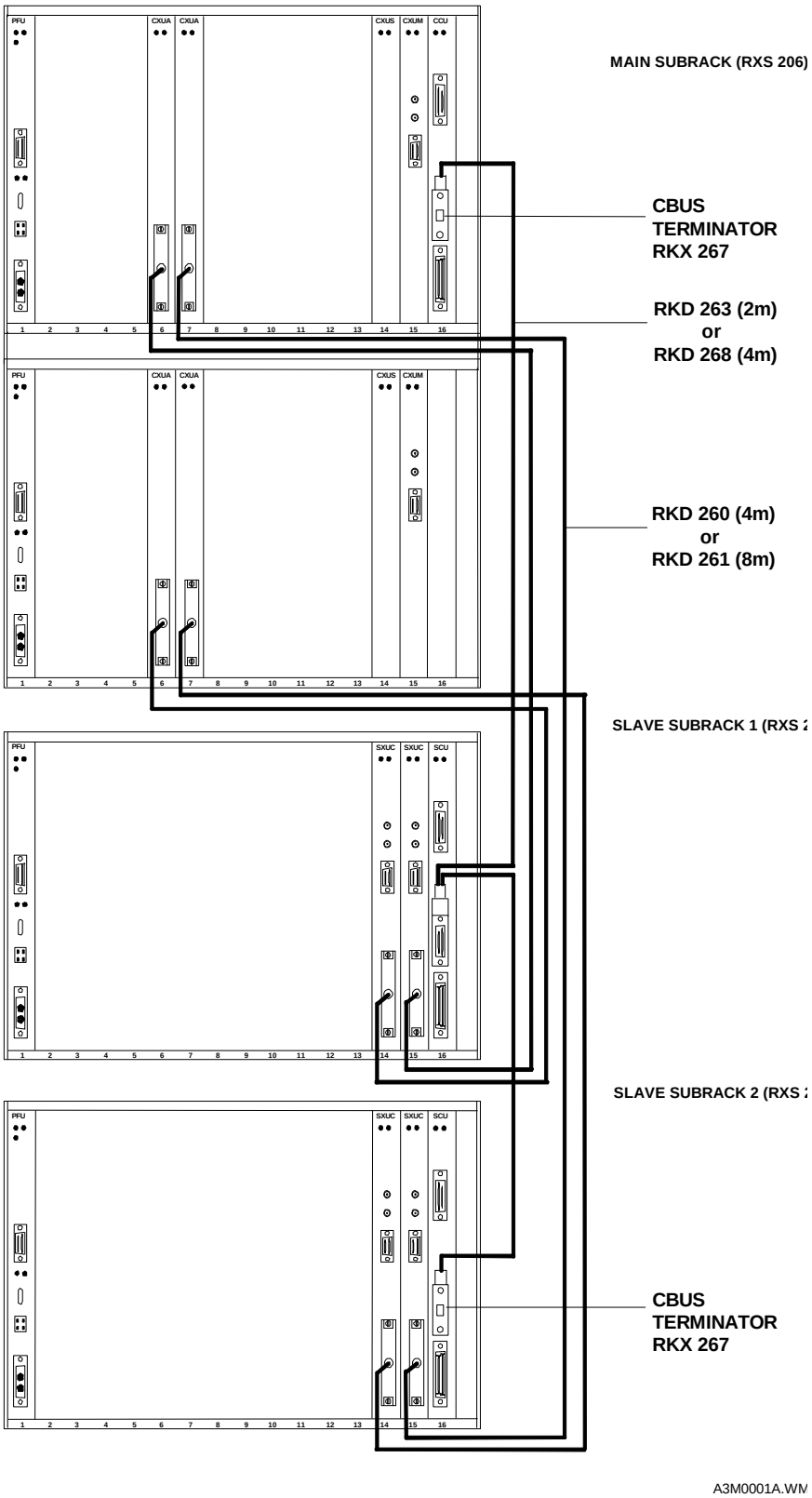


Fig. 13: Location of the Control Buses

3.4.2.3 Node-Level Operations

The SCZ 286 software installed in the CCU unit of a master subrack takes care of the following node-level operations:

- Node inventory management
- Registration of Subracks within a Cluster Node
- Subrack monitoring
- Registration of units within a master subrack
- Unit monitoring within a master subrack
- Backup of unit settings within a master subrack
- Protection of complete cross-connection system
- Protection of control buses
- Rack alarm (PMA, DMA, MEI) control
- Subrack-level summing of alarms
- Node-level summing and output of alarms
- Event reporting to the Network Management System

The SCZ 280 software installed in the SCU unit of a slave subrack takes care of the following node-level operations:

- Node inventory management
- Registration of units within a slave subrack
- Unit monitoring within a slave subrack
- Backup of unit settings within a slave subrack
- Controls activation of local SXU-Cs
- Protection of control buses of slave subrack
- Rack alarm (PMA, DMA, MEI) control
- Subrack-level summing of alarms
- Event reporting to the Network Management System
- Channel test functions
- Control channel support for the HDLC-4CH

Node Inventory Management

CCU units have the same functions for the inventory management at subrack level as SCU units. These functions include the following:

Function	Use
Identifications of node and subrack	Node parameters
Creation of inventory	Registration of all existing units for the inventory
Deletion of inventory	Unregistration of all units, i.e. removal of all units from the inventory
Addition of unit	Registration of an unit for the inventory
Removal of unit	Removal of an unit from the inventory
Inventory report on subrack level	Subrack picture (registered, existing or missing units)
Monitoring of the presence of registered or unregistered units	Fault management (see below)

The Installation Error fault condition is detected if the inventory data is not unambiguous and consistent. The Missing Unit fault condition is detected if a registered unit is not present. The Extra Unit fault condition is detected if there is an unregistered unit present in the subrack.

A Cluster Node is created by the create inventory operation applied to the master subrack with CCU and CXU-Ms and by adding CXU-As and the corresponding slave subracks. The inventory of each slave subrack must exist including SXU-C units and SCU unit before adding the corresponding CXU-As to the master subrack.

It is utmost important to make sure that all subracks have different addresses before connecting to the same cluster control bus. The slave subrack is added into a Cluster Node automatically when the corresponding CXU-A is added into the master subrack. The slave subrack is removed from the Cluster Node inventory automatically when CXU-As associated to the slave are removed from the inventory of the master subrack.

The Cluster Subracks window displays the registered and existing subracks of the Cluster Node as well as the registered as missing subracks. The Missing Subrack fault condition is detected if a registered subrack is not present.

Backup of Unit Settings

The CCU/SCU unit stores the backup settings of all registered units in the master subrack for possible unit replacements. A new replacement unit will inherit the backup settings of the unit registered for the unit slot. The compatibility of settings is checked based on the hardware and the software types.

The backup settings are updated to the CCU/SCU unit when a unit is registered or when the settings of the unit have been changed. The backup settings are copied from the CCU/SCU unit when a registered unit is replaced by another compatible unit.

The backup settings of the CCU/SCU-unit itself are kept in CXU-M/SXU-C-units. The backup of cross-connection data is available only in the redundant cross-connection units if the node has a protected cross-connection system.

Protection of Cross-Connection System

The CCU unit controls the protection of the cross-connection system. The cross-connection unit type and the protection option must be set in each subrack. These parameters are updated automatically when the inventory is created. The inventory must be deleted before changing the cross-connection unit type and recreated when the type has been changed. In the protected system the CCU unit monitors the condition of the redundant cross-connection systems and it tries to activate one of the redundant cross-connection systems if it has normal conditions. When the CCU unit makes a change-over between the redundant cross-connection systems, the following operations must take place:

— The CCU requests the CXU-Ms to disable all IS-bus interfaces
— The CCU requests all SCUs to activate the given SXU-C (1 or 2)
— The CCU requests the CXU-Ms to enable all IS-bus interfaces

The possible fault conditions for the protection of the cross-connection system are the following: The Faulty Cross-Connection System fault condition is detected if there is no cross-connection system that can be activated - both redundant cross-connection systems are faulty or missing. The Forced State in SXU/CXU Activation fault condition is detected when the protection system is not allowed to control the activation of the cross-connection systems autonomously but it is forced to keep the given state by a management operation.

Protection of Control Buses

The CCU/SCU unit controls the protection of the local VTP bus and the protection of the cluster VTP bus. The local VTP bus has two alternative physical buses called Local VTP Bus1 and Local VTP Bus2 implemented by redundant interface circuits in each DXX unit and redundant set of wires on the back plane of a subrack. There is a centralized control to activate one of the alternative buses by a selection line. The CCU/SCU unit controls the selection line in a synchronized way so that data transmission on the bus is never disturbed for the bus selection. The bus1 and the bus2 are periodically used in order to detect possible problems as soon as possible, no matter which bus will be faulty.

A checking procedure is activated when any unit has disappeared from the inventory monitoring process. The checking procedure decides whether the unit is accessible by one bus only or not. If the unit is accessible by one bus only then the other bus must be faulty and the corresponding fault condition is detected. A test window can be used to check the local VTP status and to clear the fault condition.

The cluster VTP bus has two alternative physical buses called Cluster VTP Bus1 and Cluster VTP Bus2 implemented by redundant interface circuits in each CCU/SCU unit and a redundant set of wires on the interconnection cables between the subracks of a node. There is a local control to activate one of the two receiver circuits. The data is always sent to both physical buses. The performance of physical buses is monitored and compared. When one bus is found to be worse than the other, the corresponding fault condition is detected.

Rack Alarm Control

The CCU/SCU unit controls the three LEDs and the corresponding relay outputs for the equipment alarms (PMA, DMA, MEI) of a subrack. The rack alarm LEDs and the corresponding relay outputs are located in PFU or PAU units. The rack alarms PMA, DMA, MEI are given if any unit in the subrack has an active fault condition that requires the corresponding alarm as a consequent action. The CCU/SCU unit collects PMAs, DMAs and MEIs from the units of the subrack and sums them separately for each rack alarm. The CCU unit collects PMAs, DMAs and MEIs from the SCU units of the slave subracks and sums them separately for each rack alarm in order to give rack alarms at the node level in the master subrack.

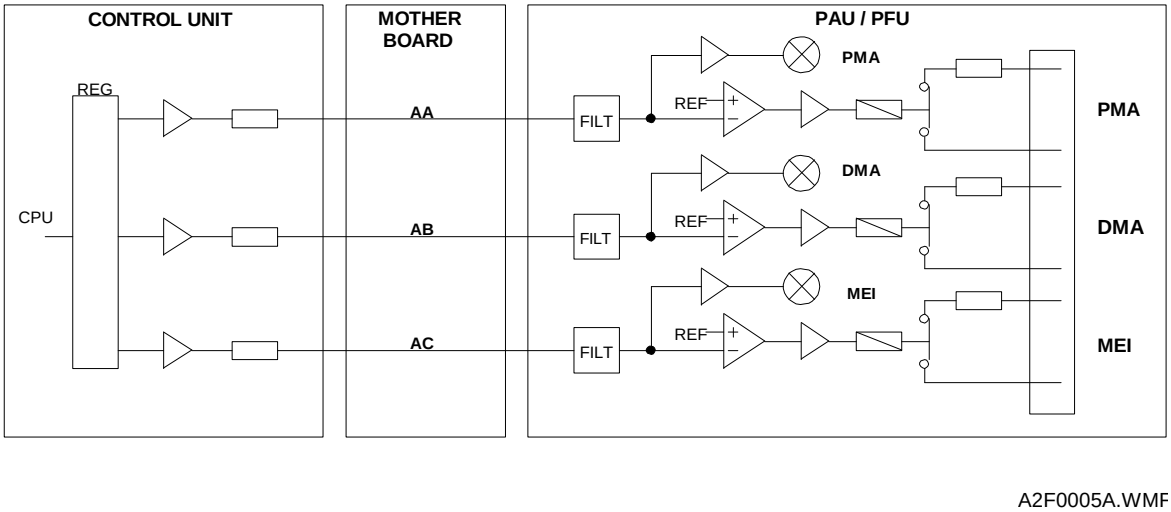


Fig. 14: Rack Alarm Control

The rack alarms can be delayed. The rack alarm delay can be set (0…600 sec) by the user. A summed alarm must be active at least the set delay time, not necessarily continuously, before the rack alarm is activated in PFU or PAU. The rack alarm will be passivated in PFU or PAU when the summed alarm has been passive continuously, at least the set delay time.

The rack alarm PMA and DMA can be cancelled. The cancellation is not delayed. When PMA and DMA have been cancelled, MEI is activated as a reminder.

Event Reporting to Network Management System

The CCU unit supervises the registered units of the master subrack and the registered slave subracks of the node. The purpose of supervision is not only the rack alarms but to support the status polling on subrack and node level from the centralized network management system as well.

The reports of node and subrack state contain the status of the subracks and units that are not in the normal state. For example, all changes in fault conditions and configuration are indicated for all units. These reports give detailed information on the correct units for different purposes.

The SCU unit supervises the registered units of the slave subrack in order to provide reports to the CCU unit of the master subrack or the management system.

While the subrack state report is created the route to the polling DXX Server is updated to the local routing table of the CCU/SCU unit from the invoke message. This route can be used to send spontaneous event reports to the DXX server. The unit reporting modules can send event report to the local CCU/SCU unit that sends them to the DXX Server. The most important application is the reporting of trunk fault changes, the trunk recovery management.

Channel Test Functions

The CCU unit does not support channel test functions in the master subrack but the SCU units in the slave subracks do.

Control Channel Support for HDLC-4CH

The CCU unit does not provide control channel support for HDLC-4CH in the master subrack but the SCU units in the slave subracks do. The bit rate of the cross-connection ports in a slave subrack can be configured to 64 kbit/s only.

3.4.3 Faults and Actions

3.4.3.1 CCU Faults

Unit Faults

Fault Condition	Status	LED	Note
Reset of Unit	PMA	R	

Power Supply Faults

Fault Condition	Status	LED	Note
VB1: + 5 V (BUS1)	DMA	R	
VB2: + 5 V (BUS2)	DMA	R	
Power + 5 V	PMA	R	
Power + 12 V	PMA	R	
Power - 10 V	PMA	R	

Memory Faults

Fault Condition	Status	LED	Note
RAM fault	PMA	R	
EPROM fault	PMA	R	
Flash memory fault	PMA	R	
Missing settings	PMA	R	
Incompatible SW in EPROM and flash	PMA	R	
Check sum error in downloaded program	PMA	R	

Control Bus Faults

Fault Condition	Status	LED	Note
Fault in Local VTP Bus1	DMA	Y	a
Fault in Local VTP Bus2	DMA	Y	a
Fault in Cluster VTP Bus1	DMA	Y	b
Fault in Cluster VTP Bus2	DMA	Y	b

a A test window can be used to check the Local VTP status and clear the fault

b Possible in a slave subrack of a Cluster Node.

Cross-Connection Protection Faults

Fault Condition	Status	LED	Note
Faulty Cross-Connection System	PMA, S	Y	a
Forced state in SXU activation	MEI	Y	

a Service alarm

Inventory Faults

Fault Condition	Status	LED	Note
Installation error	PMA, S	R	a
Missing unit	PMA, S	Y	a b
Extra unit	MEI	Y	b
Missing subrack	PMA, S	Y	a c

a Service alarm

b The block number indicates the unit address.

c The block number indicates the subrack address.

Optional External Alarms with ALARM-IF

Fault Condition	Status	LED	Note
Battery not ready	PMA	R	a
AC Off	PMA	R	b

a Contact closure in the external alarm input 1.

b Contact closure in the external alarm input 2.

3.4.4 Front Panel for CCU

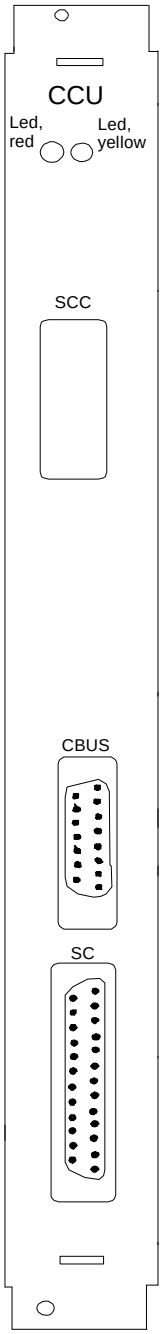


Fig. 15: CCU Front Panel (optional modules for SCC, see next page)

CCU Cluster Bus Connector (D15 Female) Pin Usage

Pin	Signal
1	Cable Shield
8	Signal Ground
6, 13	VTDT1, bidirectional
14, 7	VTCL1, bidirectional
10, 3	VTDT2, bidirectional
9, 2	VTCL2, bidirectional

CCU Local Service Computer Connector (D25 Female)

Pin	Signal
1	101 Cable Shield
2	103 transmitted data
3	104 received data
4	105 request to send
5	106 ready for sending
6	107 data set ready
7	102 signal ground
8	109 signal detector
20	108 data terminal ready
9…19	no connection
21…25	no connection

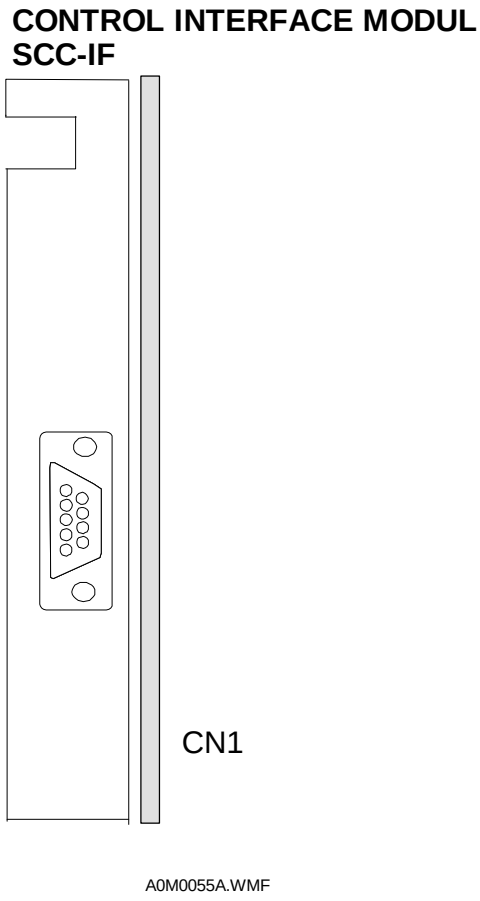


Fig. 16: Control Interface module SCC-IF

SCC-IF NMS Computer connector V.11 levels (D15 male)

Pin	Signal
1	Cable shield
2, 9	T(A), T(B), output
3, 10	C(A), C(B), output
4, 11	R(A), R(B), input
5, 12	I(A), I(B), input
6, 13	S(A), S(B), input/output
8	G, signal ground
7, 14, 15	no connection

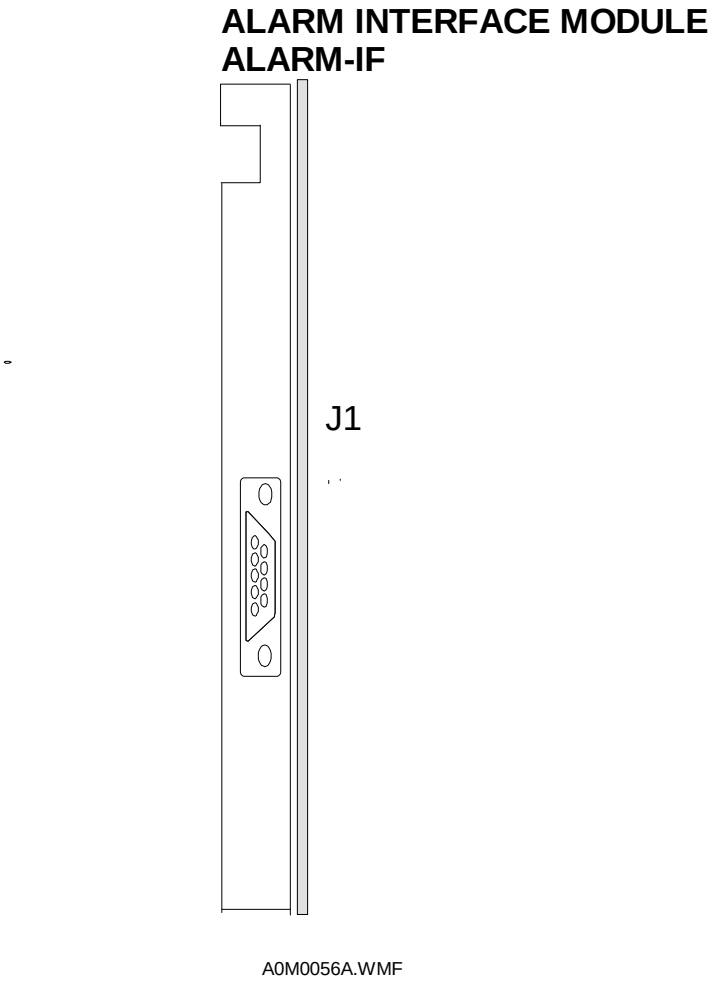


Fig. 17: Alarm Interface module Alarm-IF

Alarm Interface module pin usage (D9 female connector)

Pin	Signal
1	Contact alarm 1, input
2	No connection
3	Contact alarm 2, input
4	No connection
5	No connection
6	Return 1, signal ground
7	No connection
8	Return 2, signal ground
9	No connection

3.4.5 Cabling

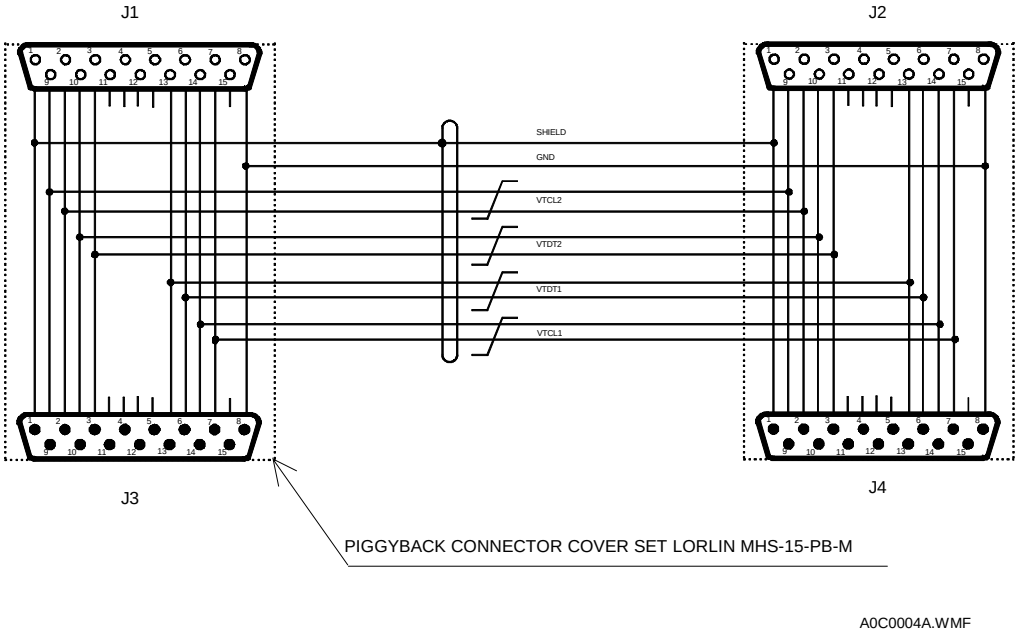


Fig. 18: CCU Control Bus Cable

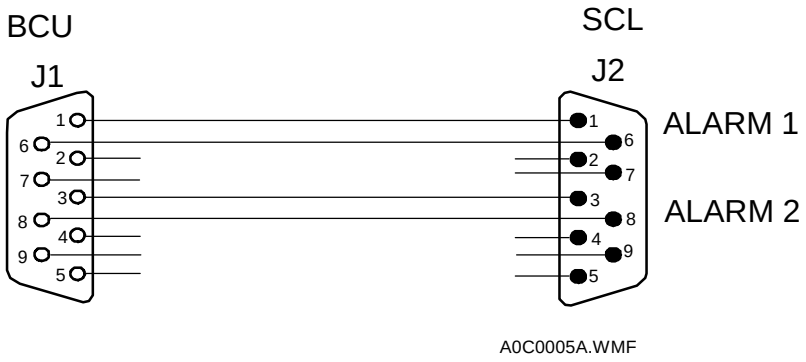


Fig. 19: BCU-SCL ALARM Interface cable

NOTE! ***Pins 6 and 8 of the connector J1 can be earthed in BCU unit if necessary.***

The same cable can also be used with the PFU-B or PFU-A.

3.4.6 Technical Specifications

3.4.6.1 Specifications of the Control Interfaces

SC Interface

Purpose	Management interface for SC/NMS
Electrical interface	V.28
Data bit rate	9600 b/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	ISO 2110, D-type 25-pin female connector
Interface signals	101, 102, 103, 104, 105, 106, 107, 108 and 109
Protocol	Layers 2…7 proprietary

SCC Interface

Purpose	Management interface for NMS
Electrical interface	V.11/X.27
Data bit rate	64 kb/s synchronous
Frame formats	F, A, C, FCS, F or F, A, C, Info, FCS, F (basic operation)
Connector type	ISO 4903, D-type 15-pin male connector
Interface signals	G, T, R, C, I, S
Protocol	LAPB + X.25 PLP + Layers 3…7 proprietary

CBUS Interface

Purpose	Cluster Control Bus
Electrical levels	V.11, redundant drivers and receivers
Data bit rate	1024 kbit/s synchronous
Connector type	ISO 4903, D-type 15-pin female connector
Interface signals	VTDT1, VTDT2 and VTCL1, VTCL2
Protocol	Layers 2…7
Physical length of the bus	20 m, maximum

3.5 Cluster Cross-Connect Unit (CXU-A)

3.5.1 General

CXU-A connects n x 64 kbit/s signals between slave subracks and within a slave subrack. CXU-A has capacity for non-blocking cross-connection in a node consisting of up to eight slave subracks.

One CXU-A (in protected mode 1 + 1) per slave subrack is mounted into the cluster main subrack. CXU-A is linked to the SXU-C of the respective slave subrack via an inter-subrack cable.

3.5.1.1 CXU-A Mechanical Structure

CXU-A consists of a base unit and modules:

— CXU 216 cluster cross-connect base unit
— CXP 217 cluster cross-connect module
— PDF 202 or PDF 209 power supply module

The power supply module is on top of the base unit along with the cross-connect module. CXU-A is 5T wide and occupies one slot in the subrack. CXU-A can be mounted into card slots 6 to 13. The slot number must correspond with the slave subrack number entered by the operator (see Cluster Node Cross-Connection description.). The connector for the intersubrack cable and the status LEDs are at the front panel.

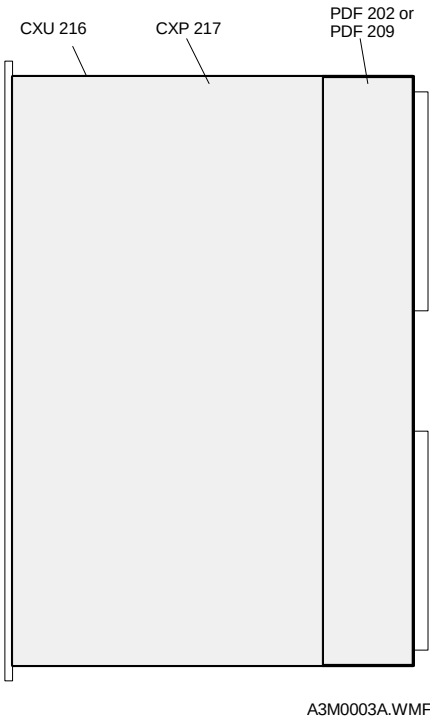


Fig. 20: CXU-A Structure

3.5.2 Operation

3.5.2.1 CXU-A Block Diagram

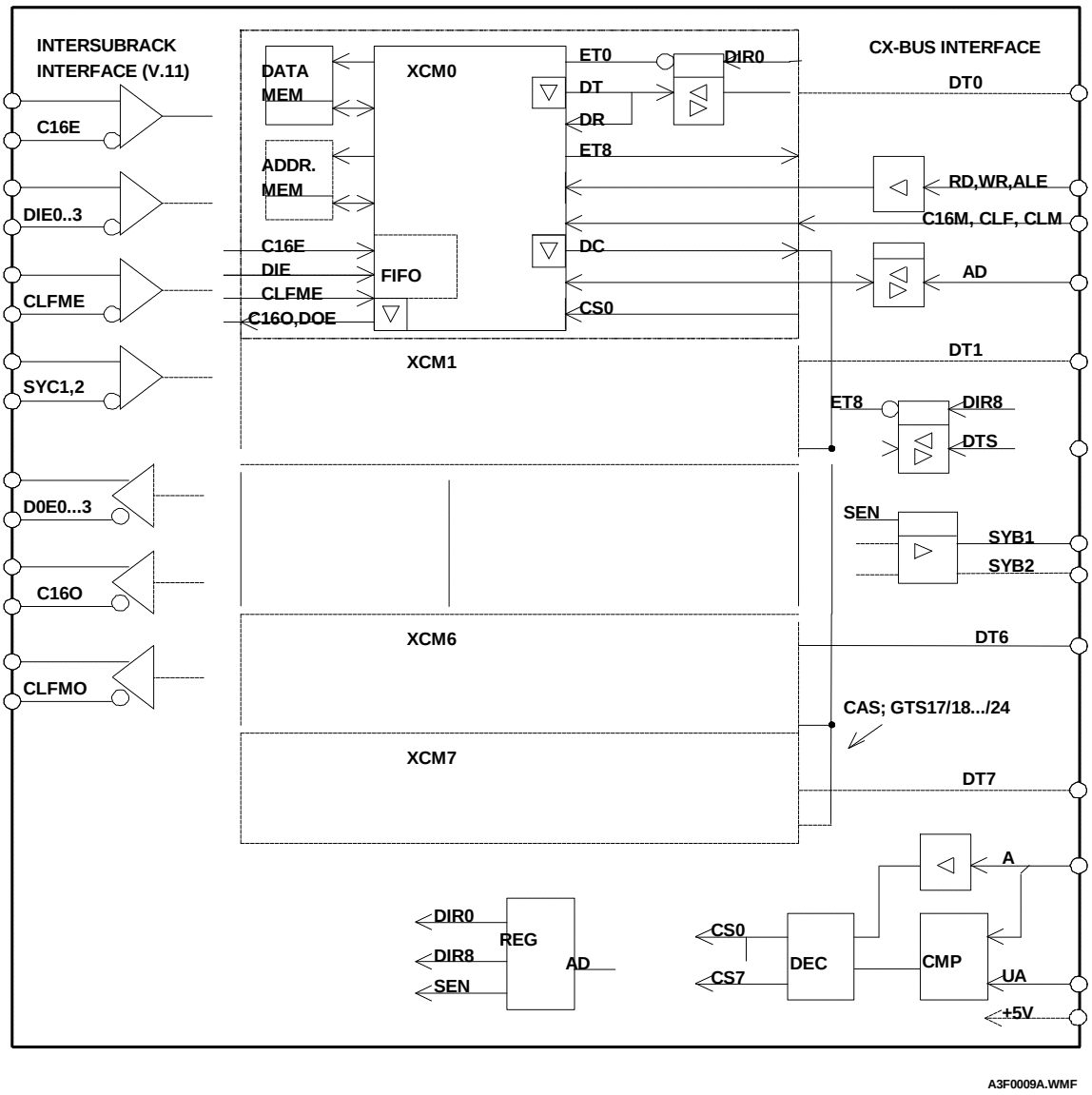


Fig. 21: CXU-A Block Diagram

3.5.2.2 Cross-Connect Matrices

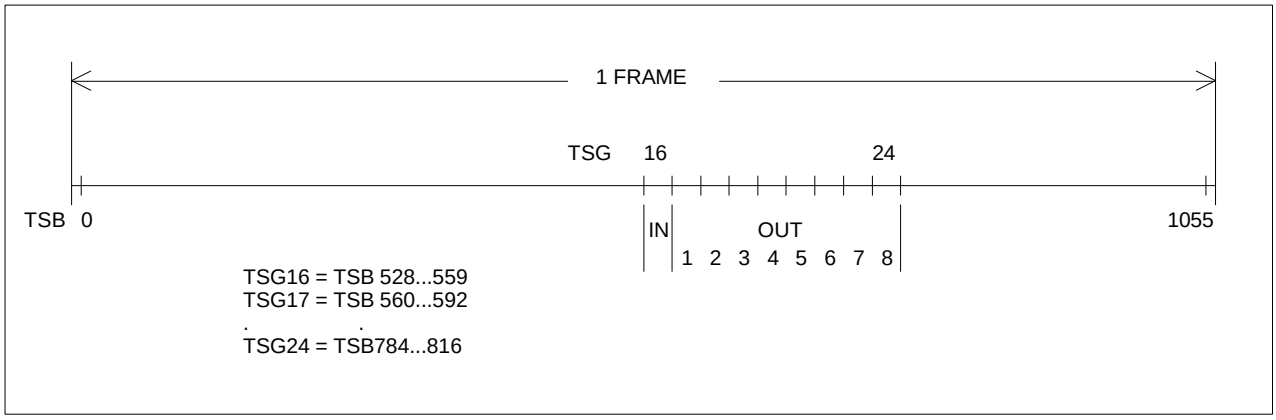
CXU-A contains eight cross-connect matrices (XCM), each with a cross-connect capacity of 67264 kbit/s. The signal from the slave subrack is stored in each XCM in a two frame buffer memory. An address memory in each XCM stores cross-connect addresses.

Every XCM has a respective cross-connect bus (DT), onto which the XCM supplies cross-connected data. XCM0 connects to DT0, XCM1 to DT1 etc. CXU-M's software assigns tasks to the correct XCM.

One of the XCMs inputs signal from its DT-bus and transfers the signal back to the slave subrack (in CXU-A/1 XCM0, in CXU-A/2 XCM1 etc).

3.5.2.3 XD Signal Buffering

CXU-A receives up to 32 time slots of XD-signals from its slave subrack. The XD-time slots are delayed by XCM0 and multiplexed to the DTS-bus during the same frame. CXU-A/0 first outputs to DTS, then CXU-A/1 and so on for a total of 256 TSs.



A3F0008A.WMF

Fig. 22: XD Signal Multiplexing onto DTS Bus

3.5.2.4 Intersubrack Interface

Fig. 21 shows the signals in the intersubrack interface. 64 Mbit/s is transmitted in both directions by four data lines and a clock and a frame/multiframe phase line.

Two reference clock signals (SYC1 and SYC2) can be brought from the slave subrack to CXU-A and enabled to the main subrack's clock bus (SYB1 and SYB2).

The signal coming from the slave subrack is written into a FIFO-buffer in every XCM. The FIFO length is adjusted to match the loop delay from CXU-A to SXU-C and back, thus maintaining the incoming signal frame phase synchronized to that of the CX-bus.

3.5.2.5 Unit Control

CXU-A is controlled by CXU-M's processor, whose data and address busses and control signals are extended to unit positions 4 to 14 via the back plane. The processor has access to CXU-A's cross-connect matrices initializing the cross-connect memories and CXU-A registers.

3.5.2.6 Power Supply

CXU-A employs the standard unit power supply module PDF 202 or PDF 209. The switching power supply provides three regulated output voltages: +5 V, + 12 V and - 10 V.

3.5.2.7 Fault Monitoring

CXU-M monitors CXU-A's cross-connect address and data memories (see CXU-M Fault Monitoring). CXU-A monitors the clock (C16E) coming from the slave subrack. Monitoring can detect a signal loss, in which case the received data is set to idle state 1.

3.5.3 CXU-A Front Panel

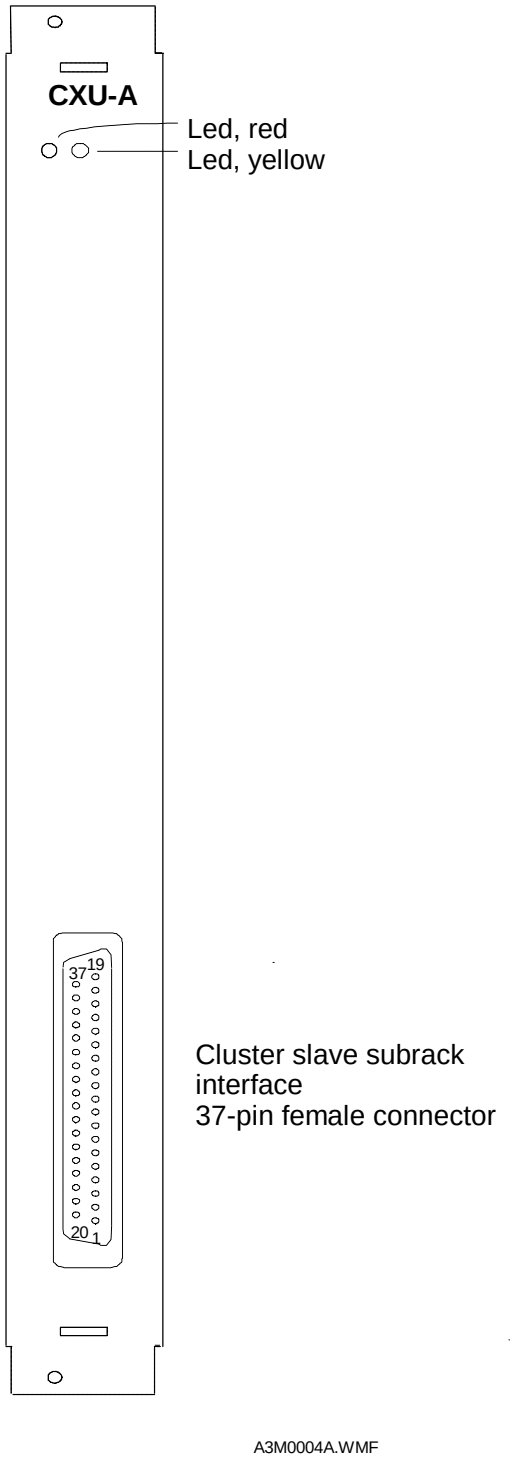


Fig. 23: CXU-A Front Panel

3.6 Cluster Signalling Cross-Connect Unit (CXU-S)

3.6.1 General

CXU-S cross-connects n x 0.5 kbit/s XD-signals. One CXU-S (in protected mode 1 + 1) is mounted into the main subrack. CXU-S has capacity for non-blocking connection in a cluster node consisting of up to eight slave subracks (8 x 2048 kbit/s of XD-channels).

3.6.1.1 CXU-S Mechanical Design

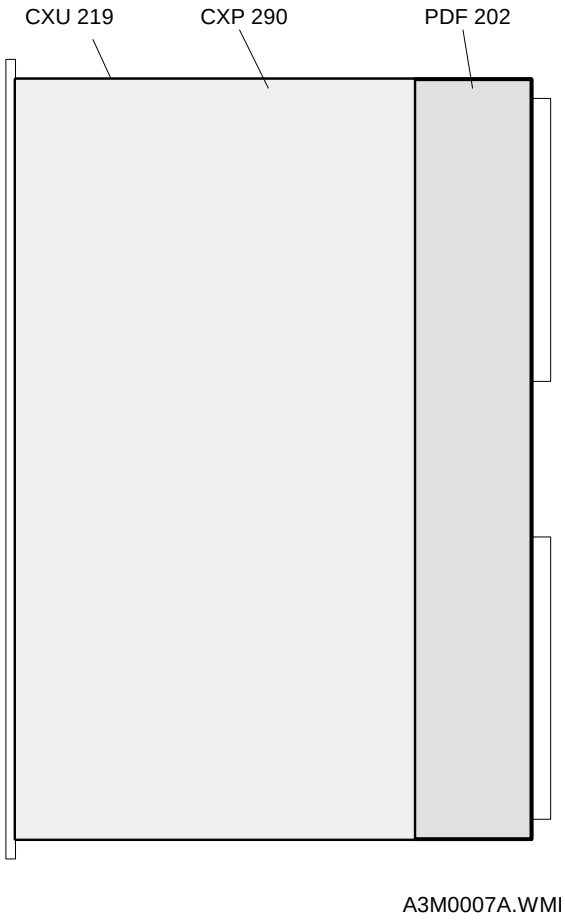


Fig. 24: CXU-S Structure

CXU-S consists of a base unit and modules:

— CXU 219 cluster cross-connect base unit
— CXP 290 cluster cross-connect module
— PDF 202 or PDF 209 power supply module

CXU-S occupies slot 14 in the cluster main subrack. Unit structure is similar to that of the CXU-A, except that there is no intersubrack connector.

3.6.2 Operation

3.6.2.1 CXU-S Block Diagram

The hardware of the CXU-S is like that of the CXU-A, but the cross-connect address memories are larger. See CXU-A description for the CXU-S block diagram.

CXU-S contains eight cross-connect matrices (XCM), each with a cross-connect capacity of 2048 kbit/s. CXU-S operation is based on the multiframe consisting of 16 frames. CXU-S receives up to 256 time slots of XD-signals in each frame via the DTS-bus. Signals are stored in a two multiframes long buffer memory in each XCM. An address memory in each XCM stores cross-connect addresses.

An XCM assembles 32 bytes in each frame bit-by-bit and stores the bytes temporarily in an intermediary buffer. Each XCM has a respective data bus (DT) in the back plane, where it supplies cross-connected data. XCM0 gives to DT0, XCM1 to DT1 and so on in time slots 528 to 559.

CXU-M software assigns tasks to the correct XCM. XCMs synchronize themselves to the clock signals at the back plane.

3.6.3 Faults

3.6.3.1 CXU-S Faults

Fault monitoring is as described in the CXU-A description.

3.6.4 Front Panel

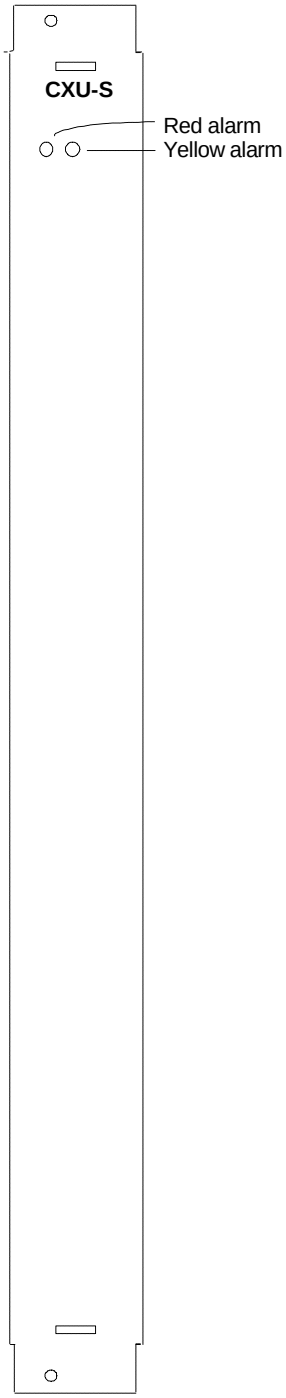


Fig. 25: CXU-S Front Panel

3.7 Cluster Cross-Connect Unit (CXU-M)

3.7.1 General

The cluster cross-connect unit CXU-M supervises the cross-connection in the cluster main subrack and supplies the subrack timing.

3.7.1.1 CXU-M Mechanical Design

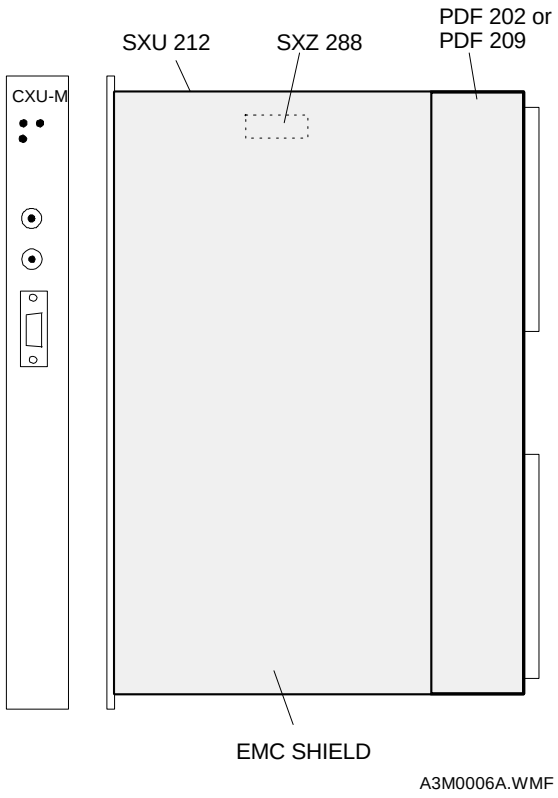


Fig. 26: CXU-M Structure

CXU-M's hardware is the same as that of the SXU-A, but the software is different. The front panel is also labelled distinctively.

CXU-M consists of a base unit and modules:

— SXU 212 cross-connect base unit
— SXZ 288 unit software module
— PDF 202 or PDF 209 power supply module

The power supply module is on top of the base unit along with an interference emission (EMC) shield. CXU-M is 5T wide and is mounted into subrack slot 15. The stand-by CXU-M is inserted into slot 15 in the lower shelf.

3.7.2 Operation

3.7.2.1 CXU-M Block Diagram

Cross-connect matrix 0 (XCM0) supplies the bus clock (16896 kHz), the frame timing (8 kHz) and the multiframe timing (0.5 kHz) to the CX-bus. XCM0 controls the phase-locked-loop 1 (PLL1) and monitors the clocks on the fall-back list.

XCM1 couples with PLL2 and supplies node clock output interface.

The two XCMs do not cross-connect in the CXU-M.

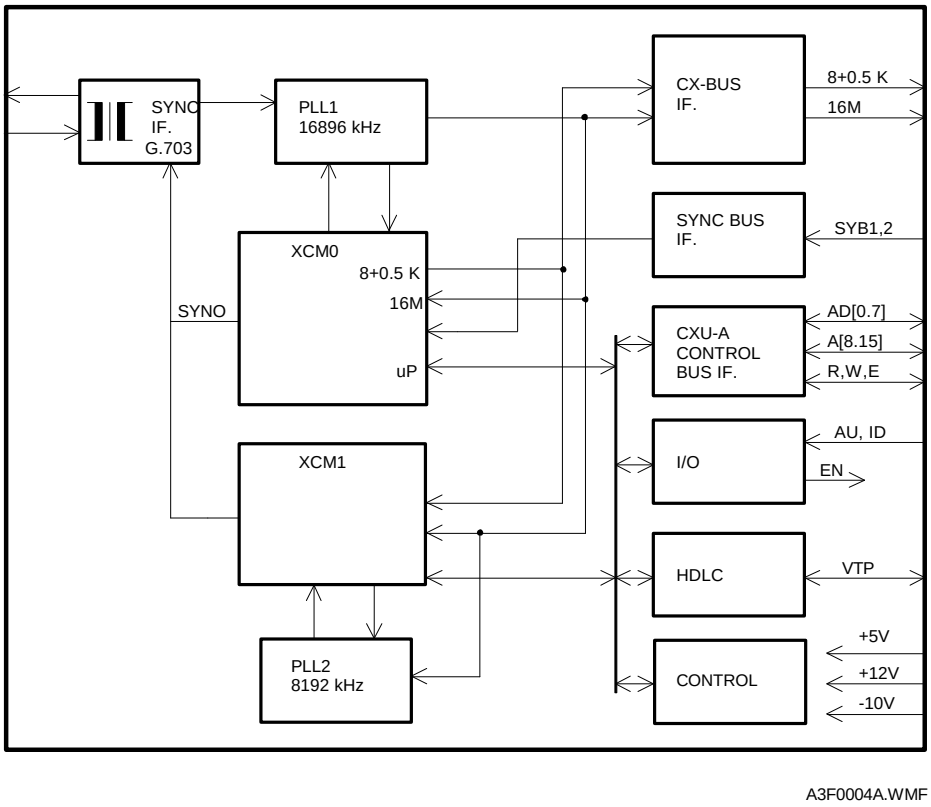


Fig. 27: CXU-M Block Diagram

Unit Control

The unit processor links to the subrack VTP-control bus via an HDLC-controller. Cross-connection commands are stored in non-volatile memories in the slave subrack SXU-Cs. The node restores its state should a power loss occur. Cross-connections can be repeatedly deleted and entered without capacity overflow.

128 kbytes of non-volatile memory is reserved for program code on the CXU-M and this part of the code can be downloaded. The core of the program code is stored in an EPROM.

A 16-bit processor runs at 16 MHz. The data and address buses of the processor have been extended to the back plane. The processor can access the cross-connect matrices and the cross-connect memories of the CXU-As without interfering with existing connections. A watchdog monitors the operation of the processor.

3.7.2.2 Node Main Oscillator

The Cluster Node's main oscillator runs at a frequency of 16896 kHz. The main oscillator can be locked to an external source, or to a received clock of an access interface (see Cluster Node clock system). For jitter and wander specifications, see “CXU-M Technical Specifications” on page 54[3.7.63.7.6]. Accuracy in internal timing mode is ± 30 ppm over the operating temperature range.

Auxiliary Oscillator

An auxiliary oscillator is locked to the main oscillator providing the node clock output interface with frequencies in the 2048 kbit/s hierarchy. Frequency of oscillation is 8192 kHz. PLL2 also supplies the 2048 kHz clock used for the VTP-control bus.

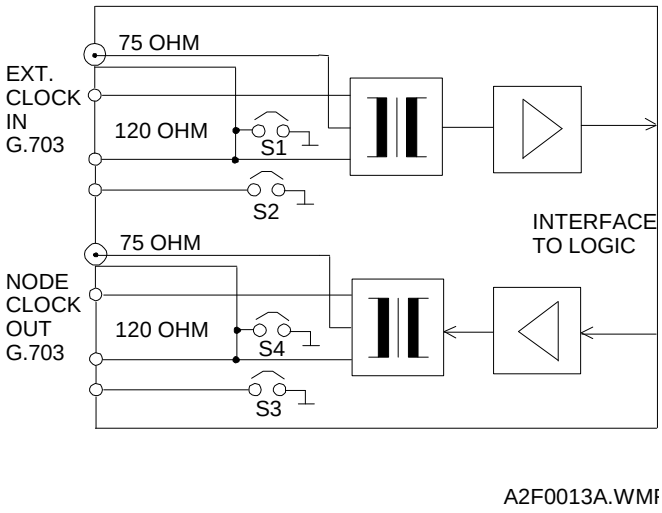


Fig. 28: Clock Interfaces

Clock Interfaces

An input interface for an external clock and an output interface for the node clock are provided. The interfaces comply with the ITU-T rec. G.703 § 10. Connectors are located in the CXU-M's front panel. For interface specifications see “CXU-M Technical Specifications” on page 54.

3.7.3 Faults

3.7.3.1 CXU-M Internal Operation Monitoring

CXU-M monitors CXU-A/CXU-S's cross-connect address memories when cross-connections are made.

The unit processor data memory, program memory and non-volatile memory are monitored.

Fault Description	Status	LED	Alarm Message
X-connect memory fault	PMA+S	Red	X-connect RAM fault, CXU-A number
X-connect matrix fault	PMA+S	Red	ASIC latch fault, CXU-A number
X-connect matrix error	MEI	-	ASIC latch warning, CXU-A number
Processor memory fault	PMA+S	Red	RAM fault
Processor program memory fault	PMA+S	Red	EPROM fault
Processor non-volatile memory fault	PMA+S	Red	Flash error

3.7.3.2 Subrack Monitoring

The CXU-M runs background tests (see Chapter Cluster Node Cross-Connections; Fault Monitoring).

3.7.3.3 Power Supply Monitoring

The CXU-M contains an analog-to-digital converter in order to monitor the unit power supply voltages. A reference voltage is provided in the CXU-M.

Fault Description	Status	LED	Alarm message
Unit supply volt. + 5/+12/-10 V out of range	PMA+S	Red	Power + 5/+12/-10 V

3.7.4 CXU-M Strapping

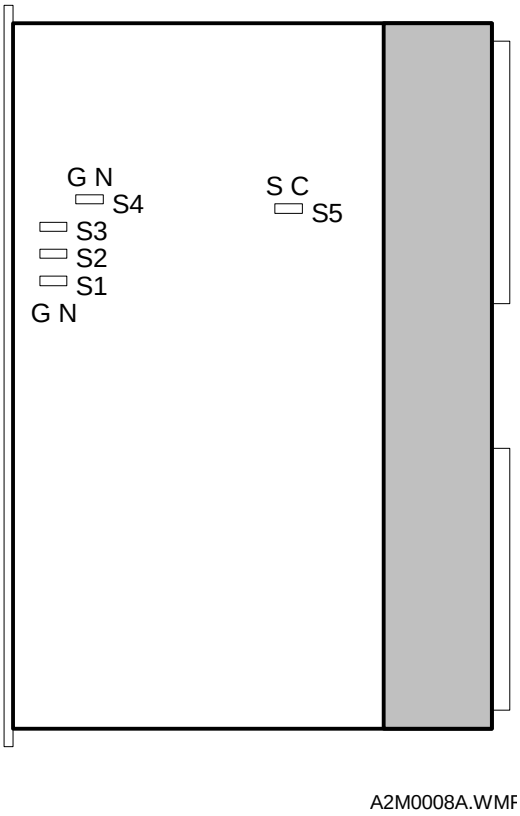


Fig. 29: Location of Straps on CXU-M

Select the coaxial (75 Ω) or the symmetrical (120 Ω) clock interface (if neither is used, the straps are irrelevant).

The ITU-T Rec. G. 703 § 10 recommends that the output cable shield is grounded and that the input shield can be grounded. Additionally the possibility to disconnect the output from ground is provided (not recommended for EMC reasons).

Coaxial Interface Used

Strap	Position	Description
S1	N	Input coaxial cable shield not grounded
	G	Input coaxial cable shield grounded
S2	*	Don't care
S3	*	Don't care
S4	N	Output coaxial cable shield not grounded
	G	Output coaxial cable shield grounded
S5	C	Always (position information to the software)

Symmetrical Interface Used

Strap	Position	Description
S1	N	Always
S2	N	Input symmetrical cable shield not grounded
	G	Input symmetrical cable shield grounded
S3	N	Output symmetrical cable shield not grounded
	G	Output symmetrical cable shield grounded
S4	N	Always
S5	S	Always (position information to the software)

3.7.5 CXU-M Front Panel

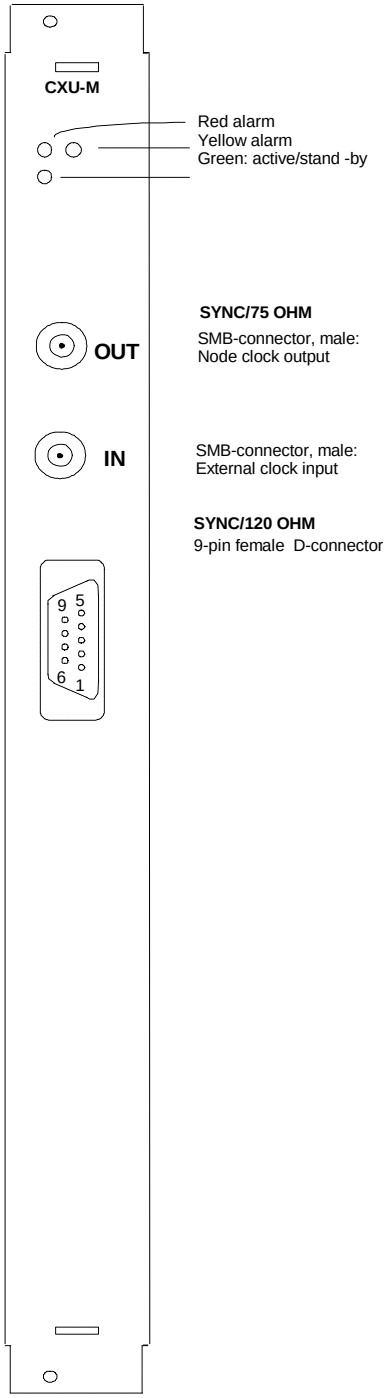


Fig. 30: CXU-M Front Panel

The front panel picture shows the LED functions. A 75 Ω coaxial interface and a 120 Ω symmetrical interface for an external clock input and the node clock output is provided. Note that only the coaxial or the symmetrical interface can be operated at a time.

Pin Usage	Signal
1	Ext. clock input, B
2	Ext. clock input, A
6	Cable shield input
3, 7, 8	GND
4	Node clock output, B
5	Node clock output, A
9	Cable shield output

3.7.6 CXU-M Technical Specifications

External Clock Input Interface (G.703 § 10.3)

Impedance	75 Ω coaxial or 120 Ω symmetrical (one at a time can be connected)
Nominal frequency	N x 64 kHz; N = 1…132
Frequency tolerance	± 50 ppm
Connector	SMB-connector male or 9-pin D-connector female
Input attenuation	6 dB at 2048 kHz max. relative to the output pulse
Input jitter tolerance	(see Node clock jitter and wander below)
Return loss	15 dB min. at 2048 kHz
Over voltage protection	G.703 Annex B with an amplitude of 50 V
Continuous signal level	5 V rms max.
Grounding	cable outer conductor can be grounded

Impedance	75 Ω coaxial or 120 Ω symmetrical, one at a time can be connected
Connector	SMB-connector male or 9-pin D-connector female
Output pulse at 2048 kHz	Figure 6 (G.703 § 10.2)
Pulse amplitude	V min = 0.75 V, V max. = 1.5 V at 75 Ω V min = 1.0 V, V max. = 1.9 V at 120 Ω
Nominal frequency	8448, 2048, 1024, 512, 256, 128, 64 kHz
Output jitter	(see Node clock jitter and wander below)
Over voltage protection	G.703 Annex B with an amplitude of 50 V
Grounding	cable outer conductor can be grounded

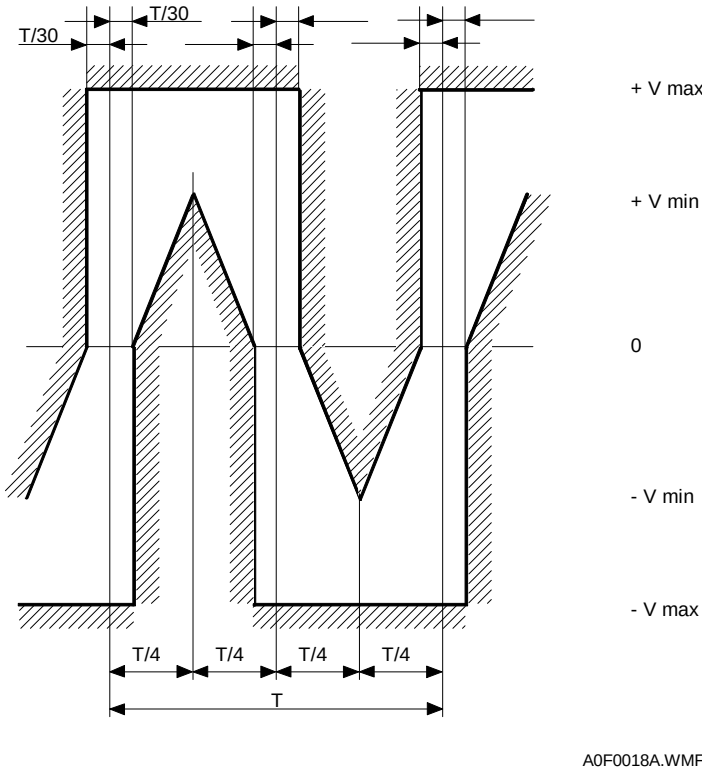


Fig. 31: Clock Output Pulse Mask at 2048 kHz

Node Clock Jitter and Wander

Output jitter, measured within the frequency range 20 Hz to 100 kHz	
2 / 8 Mbit/s and clock port output, internal timing	0.05 UIp-p max.
2 / 8 Mbit/s port output, node synchronized from an external clock at 2048 kHz containing no jitter	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an interface at 2 Mbit/s containing no jitter	0.10 UIp-p max.
8 Mbit/s port output, node synchronized from an interface at 8 Mbit/s containing no jitter	0.10 UIp-p max.

Input jitter tolerance at the external clock interface at 2048 kHz

See ": Input Jitter Tolerance for the External Clock" on page 56 (G.823 Fig. 2).

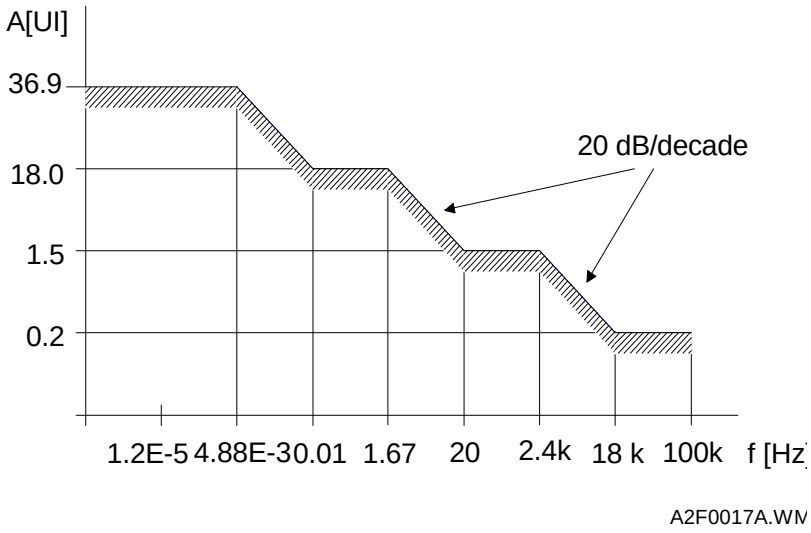


Fig. 32: Input Jitter Tolerance for the External Clock

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

See ": Jitter Transfer Function" on page 56.

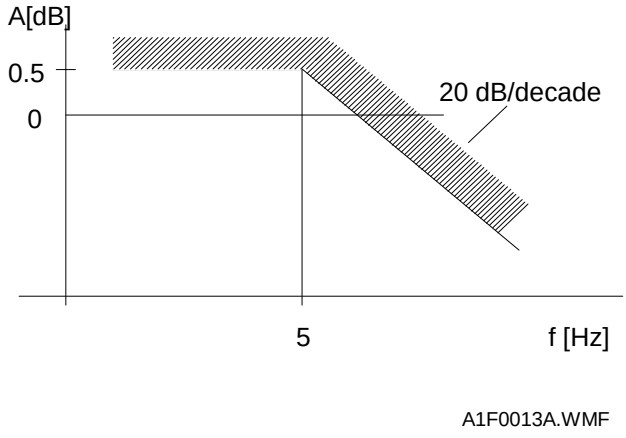


Fig. 33: Jitter Transfer Function

3.8 SXU-C Cross-Connect Unit

3.8.1 General

SXU-C is used in a Cluster Node slave subrack. It has a strictly non-blocking time-space matrix for 64 kbit/s signals. SXU-C provides n x 64 kbit/s plus XD-channel connection in a cluster node.

3.8.1.1 SXU-C Mechanical Design

SXU-C consists of a base unit and modules:

— SXU 212 cross-connect base unit
— SXZ 289 unit software module
— PDF 202 or PDF 209 power supply module
— SXP 214 cluster interface module

SXU-C is similar to SXU-A except for the cluster interface module and the unit software. The interface module links the SXU-C to the cluster main subrack via an inter-subrack cable.

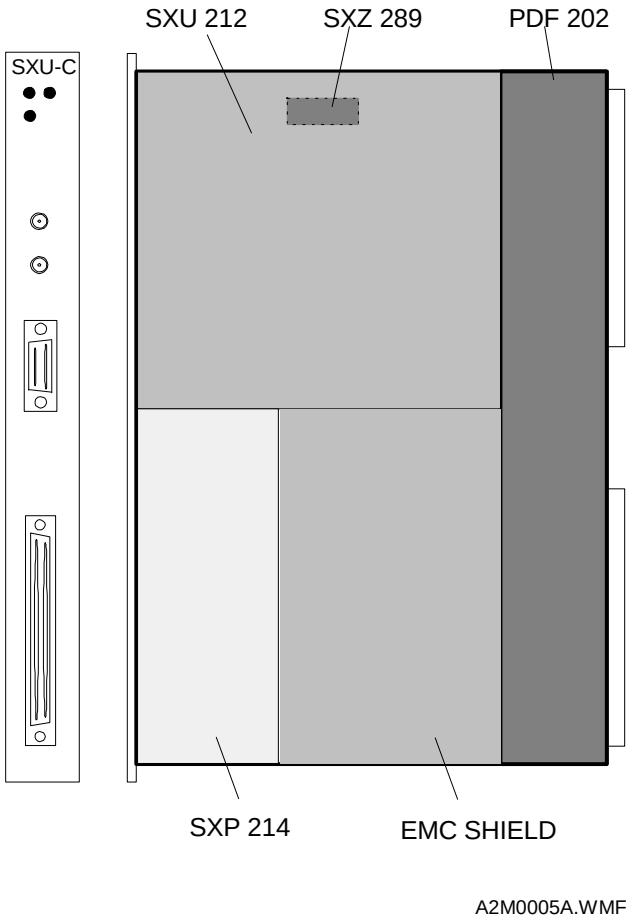


Fig. 34: SXU-C Structure

3.8.2 Operation

3.8.2.1 SXU-C Description

SXU-C consists of the base unit SXU 212 provided with a cluster interface module SXP 214. SXU-C transfers cluster slave subrack's X-bus signal to the main subrack for cross-connection. Clock and frame/multiframe synchronization is transferred with the data.

In the receive direction SXU-C cross-connect matrix 0 transfers the signal received from the main subrack interface to the X-bus. A FIFO buffer provides wander tolerance for the inter-subrack interface. XCM1 cross-connect matrix is idle in the SXU-C.

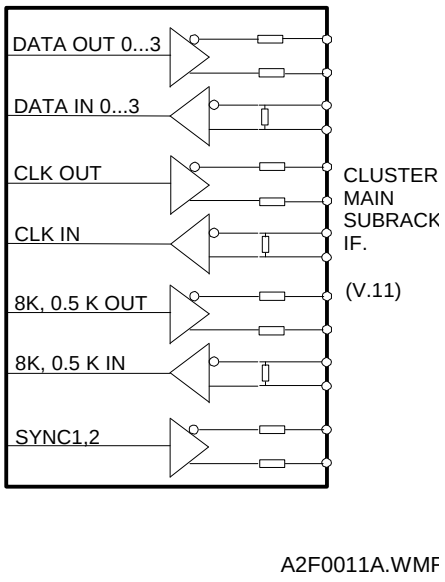


Fig. 35: SXP 214 Block Diagram

3.8.3 SXU Front Panel

Fig. 36 shows the led functions. A 75 Ω coaxial interface and a 120 Ω symmetrical interface for an external clock input and the node clock output have been provided. Either the coaxial or the symmetrical interface can be operated at a time.

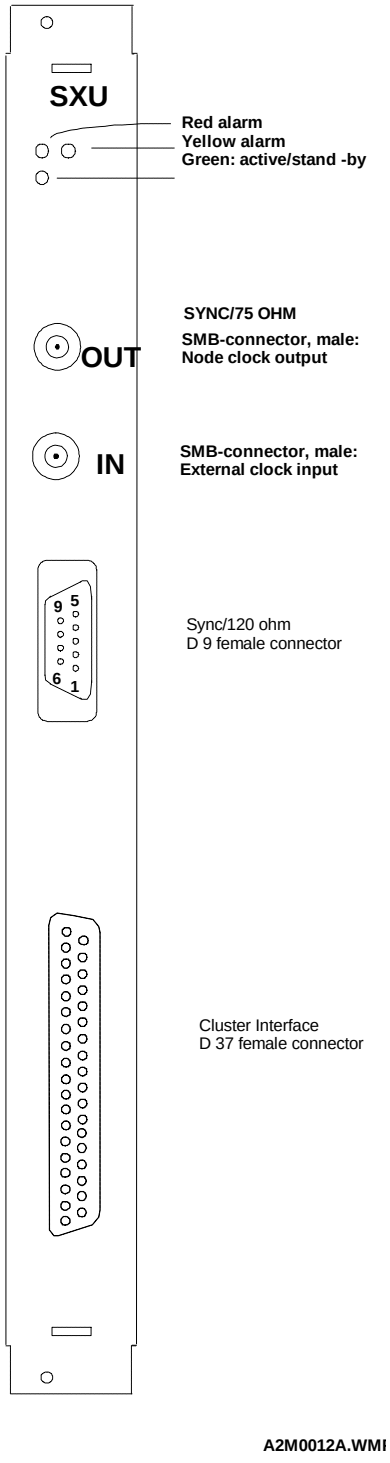


Fig. 36: SXU-C Front Panel

Pin Usage

Pin	Signal
1	Ext clock input, B
2	Ext clock input, A
6	Cable shield input
3,7,8	Gnd
4	Node clock output, B
5	Node clock output, A
9	Cable shield output

3.8.4 Cabling from SXU-C to CXU-A

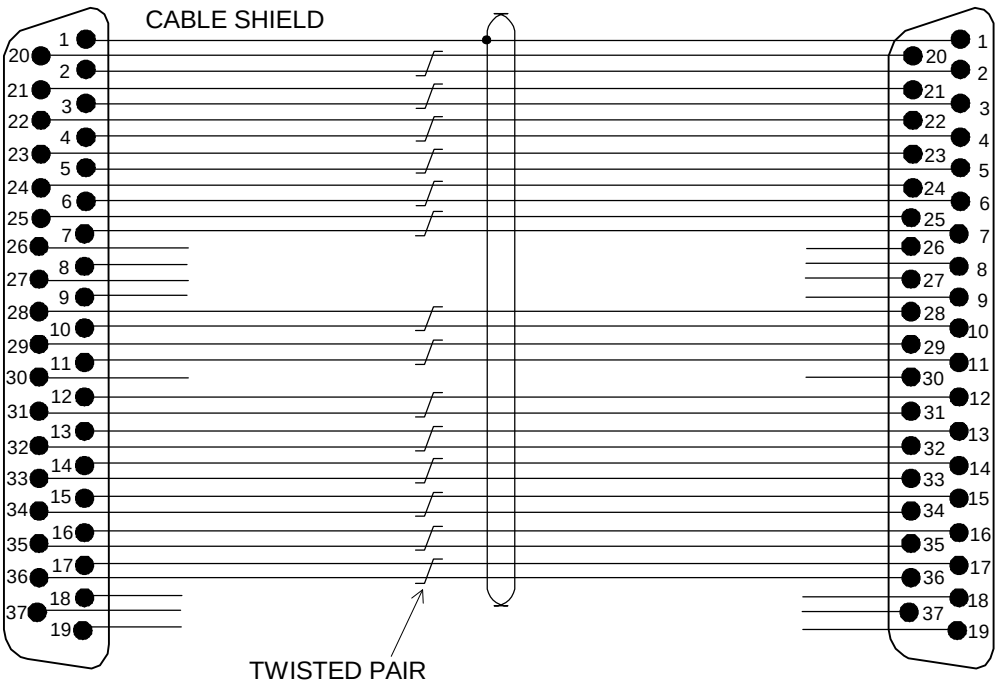


Fig. 37: Cabling from SXU-C to CXU-A